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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RA*-A0171A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Notes on IWDT refresh operation and counter read | | Information Category | Technical Notification | | |
| Applicable Product | RA8D1、RA8E1、RA8E2、RA8M1、RA8T1、RA8P1、RA8D2、RA8M2、RA8T2 | Lot No.<br>All | Reference Document | User's Manual for each product (see the table at the bottom) | | |

This document describes note on IWDT refresh operation and counter read in the above applicable products. Regarding the chapter numbers and the related table numbers for other products, refer to the chapter numbers listed in the table on the last page..

## 1. Refresh Operation

### 1.1 Note

After writing 0xFF to IWDTRR, even if the 14-bit down counter is four or more counts greater than the window end position, it may not be refreshed.

### 1.2 Cause

The refresh time after writing 0xFF to IWDTRR is described by the following formula ①:

Refresh time = 4 cycles of writing by PCLKB + 3 cycles of synchronization processing in downstream by the divided IWDTCLK ――― Formula ①

In order to complete this refresh time within 4 cycles of the divided IWDTCLK, the following conditions were set so that the 4 cycles of write by PCLKB would be less than 1 cycle of the divided IWDTCLK.

PCLKB frequency ≧ 4 × the divided IWDTCLK frequency ――― Formula ②

However, because specifications were added to the IWDT to run in deep software standby mode, a write cycle was added, and under the conditions of formula (2), the refresh time could no longer be completed in 4 cycles of the divided IWDTCLK.

### 1.3 Countermeasures

Note 1 of Table 29.1 IWDT Specifications is changed.

Before Change:

Note 1: Peripheral Module Clock (PCLKB) Frequency ≥ 4 × (Frequency of the Count Clock Source after Dividing)

After Change:

Note 1: Peripheral Module Clock (PCLKB) Frequency ≥ 32 × (Frequency of the Count Clock Source after Dividing)

2. Counter Read

2.1 Note

After returning from deep software standby mode, the 14-bit down counter value may always be read as 0.

2.2 Cause

IWDTSR.CNTVAL[13:0], which reads the counter value, is in an undefined state during deep software standby mode and is initialized by a deep software standby reset when returning from the mode.

The 14-bit down counter runs by IWDTCLK, and IWDTSR runs by PCLKB. Therefore, a synchronization circuit is inserted between them to transfer the counter value to the register, and the transfer condition is the logical OR shown below.

1. Update the count value
2. Refresh the counter

Therefore, after returning from deep software standby mode, IWDTSR.CNTVAL remains at its initial value until a transfer condition occurs, and the correct value cannot be read.

2.3 Countermeasures of issue1: Refresh Operation

The following note will be added to 29.5 Usage Notes.

29.5.2 Restrictions on Reading the Counter Value After Returning from Deep Software Standby Mode 1

After returning from Deep Software Standby Mode 1, the counter value may be read incorrectly and 0 may be read instead. To read the correct counter value after returning from Deep Software Standby Mode 1, one of the following is required:

1. Discard the read value until the counter value becomes non-zero.
2. Wait one countdown period before reading the counter value.
3. Refresh the counter when the refresh-permitted period is set to 100%.

【Reference Documents】

| Applicable Products | Related Document | Document Number | IWDT Chapter number |
|---|---|---|---|
| RA8D1 | RA8D1 Group User's Manual: Hardware Rev. 1.30 | R01UH0995EJ0130 | 26 |
| RA8E1 | RA8E1 Group User's Manual: Hardware Rev.1.10 | R01UH1129EJ0110 | 26 |
| RA8E2 | RA8E2 Group User's Manual: Hardware Rev.1.10 | R01UH1130EJ0110 | 26 |
| RA8M1 | RA8M1 Group User's Manual: Hardware Rev. 1.30 | R01UH0994EJ0130 | 26 |
| RA8T1 | RA8T1 Group User's Manual: Hardware Rev. 1.30 | R01UH1016EJ0130 | 24 |
| RA8P1 | RA8P1 Group User's Manual: Hardware Rev. 1.20 | R01UH1064EJ0120 | 29 |
| RA8T2 | RA8T2 Group User's Manual: Hardware Rev. 1.20 | R01UH1067EJ0120 | 28 |
| RA8M2 | RA8M2 Group User's Manual: Hardware Rev. 1.20 | R01UH1066EJ0120 | 28 |
| RA8D2 | RA8D2 Group User's Manual: Hardware Rev. 1.20 | R01UH1065EJ0120 | 28 |