

# RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0163A/E	Rev.	1.00
Title	Notes on running FSBL		Information Category	Technical Notification		
Applicable Product	RA8P1 Group RA8T2 Group RA8M2 Group RA8D2 Group	Lot No.	Reference Document	Hardware User Manual for each product (Refer table at the end of this document)		
		Chip version A only				

This document describes the note when running FSBL on chip version A. The page and section numbers are based on the RA8P1 Group. For other products, please refer to the table on the last page. Chip version A can be identified by reading the MCOVER.MCUVE bit in the MCU version register and confirming that it is 0x1.

## 1. Notes

In chip version A, when FSBLCTRL0.FSBLEN[2:0] is set to 000 to enable FSBL, FSBL may not operate correctly under the conditions shown in Table 7.2. Note that the conditions for external VDD mode were omitted from the table below, so we have added the information in red.

**Table 7.2 The relationship between FSBLCLK setting and system clock frequency**

System clock	FSBLCLK[2:0] = 111b (VDD = VSCR_1) (External VDD = Voltage range1)	FSBLCLK[2:0] = 110b (VDD = VSCR_1) (External VDD = Voltage range1)	FSBLCLK[2:0] = 101b (VDD = VSCR_2) (External VDD = Voltage range2)	FSBLCLK[2:0] = 100b (VDD = VSCR_2) (External VDD = Voltage range2)
CPUCLK0	250MHz	200MHz	150MHz	133MHz
CPUCLK1	250MHz	200MHz	150MHz	133MHz
ICLK	250MHz	200MHz	150MHz	133MHz
MRICK	250MHz	200MHz	150MHz	133MHz
MRPCLK	125MHz	100MHz	75MHz	66MHz
PCLKA	125MHz	100MHz	75MHz	66MHz
PCLKB	62.5MHz	50MHz	37.5MHz	33MHz
MRPCLK	125MHz	100MHz	75MHz	66MHz
PCLKA	125MHz	100MHz	75MHz	66MHz
PCLKB	62.5MHz	50MHz	37.5MHz	33MHz

Note: Other FSBLCLK settings are prohibited.

2. Reasons for malfunction

- 2.1 Under any of the conditions in Table 7.2, the SRAMWTSC.WTEN bit should have been set to 1 to add a wait state to the SRAM access cycle, but it remained 0, which may cause the SRAM to malfunction.
- 2.2 When the FSBLCLK[2:0] bits are 111b and 110b, the VSCR.VSCM[2:0] bits should have been set to 001b to set VDD to VSCR\_1 (0.95V), but they were set to 010b. As a result, VDD is set to VSCR\_2 (0.925V), which may cause malfunction.
- 2.3 When FSBL is running, the HOCO clock source for PLL1 is set to 24MHz. However, depending on the frequency deviation of the HOCO, each clock frequency generated from the frequency multiplied by PLLCCR.PLLMUL[8:0] may exceed its maximum value.

3. Countermeasure

In chip version A, do not enable FSBL by setting FSBLCTRL0.FSBLEN[2:0] to 000.

- 4. Regarding the differences in specifications by chip version, The following has been added to Table 1.1 on page 4 for all products.

Table 1.1: Differences in Specifications by Chip Version

Chapter		Specification Differences	
		Chip version A	Chip version B
7. Option-Setting Memory	7.2.11 FSBLCTRL0 FSBL Control Register 0	Setting the FSBLEN[2:0] bits to 000b is prohibited	Setting the FSBLEN[2:0] bits to 000b is permitted.

**[Reference document]**

Applicable Product	Manual Title	Document Number	Page Number	Section Number
RA8P1	RA8P1 Group User’s Manual: Hardware Rev.1.20	R01UH1064EJ0120	294 of 4294	7.2.11
RA8T2	RA8T2 Group User’s Manual: Hardware Rev.1.20	R01UH1067EJ0120	278 of 3699	7.2.11
RA8M2	RA8M2 Group User’s Manual: Hardware Rev.1.20	R01UH1066EJ0120	281 of 3896	7.2.11
RA8D2	RA8D2 Group User’s Manual: Hardware Rev.1.20	R01UH1065EJ0120	293 of 4279	7.2.11