To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-505A/EA	Rev.	1.0
Title	Notice of Scan mode and Multi mode of A/D conversion		Information Category	Usage Limitation		
Applicable Product	SH7760	Lot No. All	Reference Document	SH7760 hardware manual (ADE-602-291)		

The A/D Converter (ADC) of SH7760 has following notice.

1. Condition

There is the case of stopping or NOT starting of A/D conversion in SCAN mode or MULTI mode, because ADC can not detect the changing of ADST when the period of ADST changing is shorter than the sampling period of the clock cycle selected with CKSL1,0.

For example, the A/D convertion may not be started depending on the setting timing of ADST, even though ADST is set to 1(ADST=1) to start the A/D conversion again after the A/D start bit (ADCSR.ADST = 0) was cleared to stop conversion during the A/D operation.

2. Workaround

It is possible to evade by the method of following (1) or (2).

(1)When ADC is used in SCAN mode, or ADC is stopped AD conversion by ADST=0 during AD operation (ADCSR.ADF=0) in MULTI mode, please set ADST to 1 after an interval of AD convertion time shown table 1 from the time of setting ADST=0.

Table 1 AD Conversion Time

	Pck / 4	Pck / 8	Pck / 16	Pck / 32
AD Conversion Time	134	266	530	1058

Unit[cycle]

(2)Please leave it longer than the 1 cycle of the selected clock with CKSL1,0(Table 2) of the A/D Control/Status Register(ADCSR) according to Pck in Table 3 and the setting of the clock dividing frequency.

Table 2 ADST transitoin period

	ADCSR.CKSL1, 0			
	2'b00	2'b01	2'b10	2'b11
ADST transitoin period [sec]	4 / Pck	8 / Pck	16 / Pck	32 / Pck

Table 3 Setting between Pck and Clock Division Ratio

Clock Division Ratio	Pck
Pck / 4	Less than 18MHz.
Pck / 8	Less than 34MHz
Pck / 16	Less than 34MHz
Pck / 32	Less than 34MHz