

# RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan  
Renesas Electronics Corporation

Product Category	MPU/MCU	Document No.	TN-RA*-A0173A/E	Rev.	1.00
Title	RA0E1 Description in the User's Manual: Hardware, Changed.		Information Category	Technical Notification	
Applicable Product	RA0E1 Group	Lot No.	Reference Document	RA0E1 Group User's Manual: Hardware Rev.1.20 (R01UH1040EJ0120)	
		All			

This document describes misstatements found in the RA0E1 User's Manual: Hardware (hereinafter "UM"), Rev. 1.20 (R01UH1040EJ0120).

## Corrections

Applicable Item	UM Applicable Page	Contents	Pages in this document for corrections
Features	Page 24	addition	Page 2
Table 1.11 I/O ports	Page 28	addition	Page 3
Table 1.13 Function comparison	Page 32	addition	Page 4,5
Figure 1.5 Pin assignment for LSSOP/TSSOP 20-pin (top view)	Page 36	Caution added	Page 6
Table 1.15 Pin list	Page 38	Caution added	Page 7,8
Figure 8.2 Clock generation circuit block diagram (24-, 20-, 16-pin)	Page 76	Caution added	Page 9,10
Table 8.3 Clock generation circuit input/output pins			
8.2.1 CMC : Clock Operation Mode Control Register	Page 76,77	Caution added	Page 11,12
8.2.2 SOMRG : Sub-clock Oscillator Margin Check Register	Page 78	Caution added	Page 13
8.2.5 FSUBSCR : FSUB Clock Source Control Register	Page 79	Caution added	Page 14
8.2.8 SOSCCR : Sub-clock Oscillator Control Register	Page 81	Caution added	Page 15
8.2.18 OSMC : Subsystem Clock Supply Mode Control Register	Page 89	Caution added	Page 16
8.4 Sub-clock Oscillator	Page 93	Caution added	Page 17
Table 18.1 Specifications of 32-bit interval timer operations	Page 285	Caution added	Page 17,18
Table 19.1 RTC specifications	Page 302	Caution added	Page 19
Table 23.1 UARTA specifications	Page 526	Caution added	Page 20
Table 25.1 ADC12 specifications (2 of 2)	Page 556	addition	Page 21
Sub-clock Oscillator Characteristics	Page 665	Caution added	Page 22
Table 31.40 A/D conversion characteristics in Normal modes 1 and 2	Page 709	Caution added	Page 23,24
Table 31.41 A/D conversion characteristics in Low-voltage modes 1 and 2	Page 709, 710	Caution added	Page 25,26,27
Table 31.42 A/D conversion characteristics in Low-voltage modes 1 and 2	Page 710, 711	Caution added	Page 28,29

## Document Improvement

The above corrections will be made for the next revision of the UM.

**[Before correction of Features] (UM P24)**

■ Arm Cortex-M23 Core

- Armv8-M architecture
- Maximum operating frequency: 32 MHz
- Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

■ Memory

- Up to 64-KB code flash memory
- 1-KB data flash memory (1,000,000 (TYP) program/erase cycles)
- 12-KB SRAM
- Flash read protection (FRP)
- 128-bit unique ID

■ Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 32-pin HWQFN (5 mm × 5 mm, 0.5 mm pitch)
  - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
  - 20-pin LSSOP (4.4 mm × 6.5 mm, 0.65 mm pitch)
  - 16-pin HWQFN (3 mm × 3 mm, 0.5 mm pitch)

**[After correction of Features] (UM P24)**

■ Arm Cortex-M23 Core

- Armv8-M architecture
- Maximum operating frequency: 32 MHz
- Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

■ Memory

- Up to 64-KB code flash memory
- 1-KB data flash memory (1,000,000 (TYP) program/erase cycles)
- 12-KB SRAM
- Flash read protection (FRP)
- 128-bit unique ID

■ Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 32-pin HWQFN (5 mm × 5 mm, 0.5 mm pitch)
  - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
  - 20-pin LSSOP (4.4 mm × 6.5 mm, 0.65 mm pitch)
  - **20-pin TSSOP (4.4 mm × 6.5 mm, 0.65 mm pitch)**
  - 16-pin HWQFN (3 mm × 3 mm, 0.5 mm pitch)

[Before correction of Table 1.11 I/O ports] (UM P28)

Feature	Functional description
I/O ports	<ul style="list-style-type: none"> <li>● I/O ports for the 32-pin LQFP/HWQFN                             <ul style="list-style-type: none"> <li>– I/O pins: 26</li> <li>– Input pins: 3</li> <li>– Pull-up resistors: 16</li> <li>– N-ch open-drain outputs: 15</li> <li>– 5-V tolerance: 2</li> </ul> </li> <li>● I/O ports for the 24-pin HWQFN                             <ul style="list-style-type: none"> <li>– I/O pins: 20</li> <li>– Input pins: 1</li> <li>– Pull-up resistors: 12</li> <li>– N-ch open-drain outputs: 11</li> <li>– 5-V tolerance: 2</li> </ul> </li> <li>● I/O ports for the 20-pin LSSOP                             <ul style="list-style-type: none"> <li>– I/O pins: 16</li> <li>– Input pins: 1</li> <li>– Pull-up resistors: 12</li> <li>– N-ch open-drain outputs: 9</li> </ul> </li> <li>● I/O ports for the 16-pin HWQFN                             <ul style="list-style-type: none"> <li>– I/O pins: 12</li> <li>– Input pins: 1</li> <li>– Pull-up resistors: 9</li> <li>– N-ch open-drain outputs: 6</li> </ul> </li> </ul>

[After correction of Table 1.11 I/O ports] (UM P28)

Feature	Functional description
I/O ports	<ul style="list-style-type: none"> <li>● I/O ports for the 32-pin LQFP/HWQFN                             <ul style="list-style-type: none"> <li>– I/O pins: 26</li> <li>– Input pins: 3</li> <li>– Pull-up resistors: 16</li> <li>– N-ch open-drain outputs: 15</li> <li>– 5-V tolerance: 2</li> </ul> </li> <li>● I/O ports for the 24-pin HWQFN                             <ul style="list-style-type: none"> <li>– I/O pins: 20</li> <li>– Input pins: 1</li> <li>– Pull-up resistors: 12</li> <li>– N-ch open-drain outputs: 11</li> <li>– 5-V tolerance: 2</li> </ul> </li> <li>● I/O ports for the 20-pin LSSOP/TSSOP                             <ul style="list-style-type: none"> <li>– I/O pins: 16</li> <li>– Input pins: 1</li> <li>– Pull-up resistors: 12</li> <li>– N-ch open-drain outputs: 9</li> </ul> </li> <li>● I/O ports for the 16-pin HWQFN                             <ul style="list-style-type: none"> <li>– I/O pins: 12</li> <li>– Input pins: 1</li> <li>– Pull-up resistors: 9</li> <li>– N-ch open-drain outputs: 6</li> </ul> </li> </ul>

[Before correction of Table 1.13 Function comparison] (UM P32)

Parts number		R7FA0E1073CFJ R7FA0E1073CNH	R7FA0E1053CFJ R7FA0E1053CNH	R7FA0E1073CNK	R7FA0E1053CNK	R7FA0E1073CSC R7FA0E1073CSD	R7FA0E1053CSC	R7FA0E1073CNL	R7FA0E1053CNL
Pin count		32		24		20		16	
Package		LQFP/HWQFN		HWQFN		LSSOP/ TSSOP	LSSOP	HWQFN	
Code flash memory		64 KB	32 KB	64 KB	32 KB	64 KB	32 KB	64 KB	32 KB
Data flash memory		1 KB		1 KB		1 KB		1 KB	
SRAM (Parity)		12 KB		12 KB		12 KB		12 KB	
System	CPU clock	32 MHz		32 MHz		32 MHz		32 MHz	
	Sub-clock oscillator	Yes		Yes (CMC.XTSEL=1)		Yes (CMC.XTSEL=1)		Yes (CMC.XTSEL=1)	
	ICU	Yes		Yes		Yes		Yes	
Event control	ELC	Yes		Yes		Yes		Yes	
DMA	DTC	Yes		Yes		Yes		Yes	
Timers	TAU	8 (PWM outputs: 7)		8 (PWM outputs: 7)		8 (PWM outputs: 7)		8 (PWM outputs: 7)	
	TML32	1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)		1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)		1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)		1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)	
	RTC	Yes		Yes		Yes		Yes	
	IWDT	Yes		Yes		Yes		Yes	
Communication	SAU <sup>1</sup>	3 (simplified SPI), 3 (simplified IIC), 2 (UART), 1 (UART supporting LIN-bus)		3 (simplified SPI), 3 (simplified IIC), 2 (UART), 1 (UART supporting LIN-bus)		3 (simplified SPI), 3 (simplified IIC), 2 (UART), 1 (UART supporting LIN-bus)		2 (simplified SPI), 2 (simplified IIC), 2 (UART)	
	UARTA	1		1		1		1	
	IICA	1		1		1		1	
Analog	ADC12	10		8		6		5	
	TSN	Yes		Yes		Yes		Yes	
Data processing	CRC	Yes		Yes		Yes		Yes	
Security		TRNG		TRNG		TRNG		TRNG	
I/O ports	I/O pins	26		20		16		12	
	Input pins	3		1		1		1	
	Pull-up resistors	16		12		12		9	
	N-ch open-drain outputs	15		11		9		6	
	5-V tolerance	2		2		—		—	

Note 1. SAU consists of several channels. Each channel can be assigned only one function at a time.

[After correction of Table 1.13 Function comparison] (UM P32)

Parts number		R7FA0E1073CFJ R7FA0E1073CNH	R7FA0E1053CFJ R7FA0E1053CNH	R7FA0E1073CNK	R7FA0E1053CNK	R7FA0E1073CSD	R7FA0E1073CSC	R7FA0E1053CSC	R7FA0E1073CNL	R7FA0E1053CNL
Pin count		32		24		20			16	
Package		LQFP/HWQFN		HWQFN		TSSOP	LSSOP		HWQFN	
Code flash memory		64 KB	32 KB	64 KB	32 KB	64KB	64 KB	32 KB	64 KB	32 KB
Data flash memory		1 KB		1 KB		1KB			1 KB	
SRAM (Parity)		12 KB		12 KB		12KB			12 KB	
System	CPU clock	32 MHz		32 MHz		32 MHz			32 MHz	
	Sub-clock oscillator	Yes		Yes (CMC.XTSEL=1)		No	Yes (CMC.XTSEL=1)		Yes (CMC.XTSEL=1)	
	ICU	Yes		Yes		Yes			Yes	
Event control	ELC	Yes		Yes		Yes			Yes	
DMA	DTC	Yes		Yes		Yes			Yes	
Timers	TAU	8 (PWM outputs: 7)		8 (PWM outputs: 7)		8 (PWM outputs: 7)			8 (PWM outputs: 7)	
	TML32	1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)		1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)		1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)			1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)	
	RTC	Yes		Yes		Yes			Yes	
	IWDT	Yes		Yes		Yes			Yes	
Communication	SAU*1	3 (simplified SPI), 3 (simplified IIC), 2 (UART), 1 (UART supporting LIN-bus)		3 (simplified SPI), 3 (simplified IIC), 2 (UART), 1 (UART supporting LIN-bus)		3 (simplified SPI), 3 (simplified IIC), 2 (UART), 1 (UART supporting LIN-bus)			2 (simplified SPI), 2 (simplified IIC), 2 (UART)	
	UARTA	1		1		1			1	
	IICA	1		1		1			1	
Analog	ADC12	10		8		6			5	
	TSN	Yes		Yes		Yes			Yes	
Data processing	CRC	Yes		Yes		Yes			Yes	
Security		TRNG		TRNG		TRNG			TRNG	
I/O ports	I/O pins	26		20		16			12	
	Input pins	3		1		1			1	
	Pull-up resistors	16		12		12			9	
	N-ch open-drain outputs	15		11		9			6	
	5-V tolerance	2		2		—			—	

Note 1. SAU consists of several channels. Each channel can be assigned only one function at a time.

[Before correction of Figure 1.5 Pin assignment for LSSOP/TSSOP 20-pin (top view)]

(UM P36)

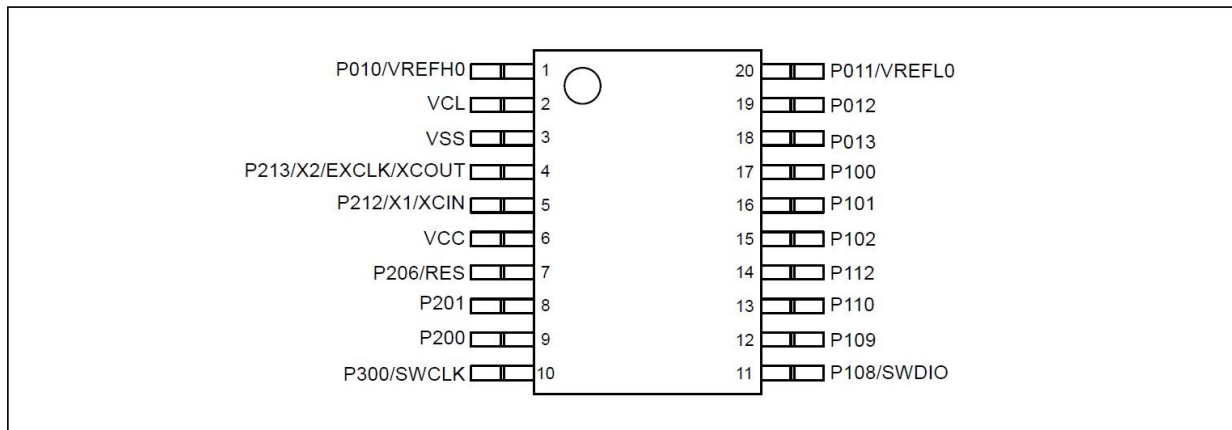


Figure 1.5 Pin assignment for LSSOP/TSSOP 20-pin (top view)

[After correction of Figure 1.5 Pin assignment for LSSOP/TSSOP 20-pin (top view)]

(UM P36)

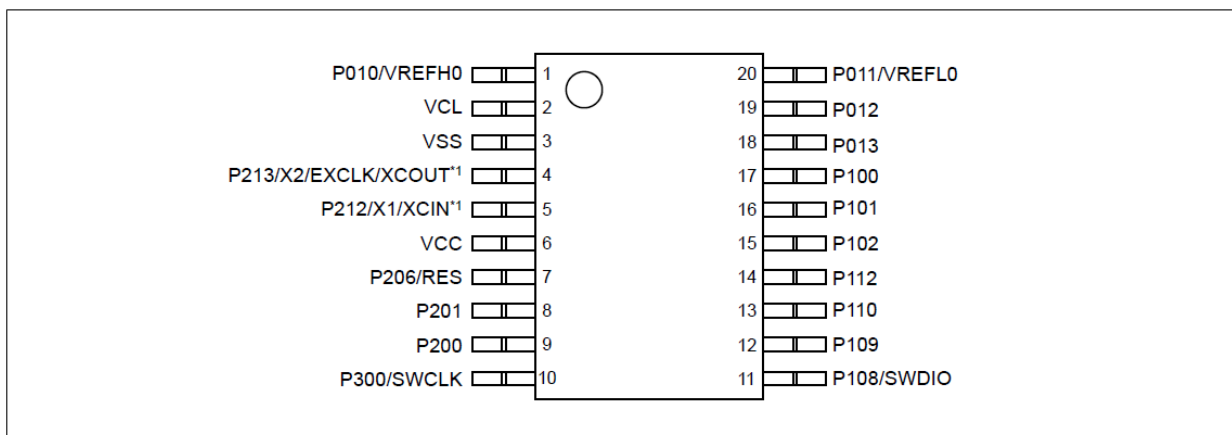


Figure 1.5 Pin assignment for LSSOP/TSSOP 20-pin (top view)

Note. Not available on the 20-pin TSSOP product.

[Before correction of Table 1.15 Pin list] (UM P38)

Pin number				Power, System, Clock, Debug	I/O ports	Interrupt	Timers		Communication interfaces			Analogs
32-pin	24-pin	20-pin	16-pin				TAU	RTC	SAU	IICA	UARTA	ADC
1	1	2	16	VCL	—	—	—	—	—	—	—	—
2	—	—	—	XCIN	P215	—	—	—	—	—	—	—
3	—	—	—	XCOUT	P214	—	—	—	—	—	—	—
4	2	3	1	VSS	—	—	—	—	—	—	—	—
5	3	4	2	X2/EXCLK/ XCOUT <sup>*1</sup>	P213	IRQ0_B	Ti00_A/Ti02_B/ TO02_B	—	TXD1_A/ SO11_A	SDAA0_B	TXDA0_B	—
6	4	5	3	X1/XCIN <sup>*1</sup>	P212	IRQ1_B	TO00_A/ Ti03_C/TO03_C	—	RXD1_A/ SI11_A/ SDA11_A	SCLA0_B	RXDA0_B	—
7	5	6	4	VCC	—	—	—	—	—	—	—	—
8	—	—	—	PCLBUZ0_C	P407	IRQ4_C	—	RTCCOUT_A	SCK11_A/ SCL11_A	—	—	—
9	6	—	—	—	P914	—	—	—	SCLA0_A	—	—	—
10	7	—	—	—	P913	—	—	—	SDAA0_A	—	—	—
11	—	—	—	—	P208	IRQ3_C	Ti00_B	—	—	—	TXDA0_A	—
12	—	—	—	—	P207	IRQ2_C	TO00_B	—	—	—	RXDA0_A	—
13	8	7	5	RES	P206	—	—	—	—	—	—	—
14	9	8	6	PCLBUZ0_A	P201	IRQ5_B	Ti05_B/TO05_B	RTCCOUT_B	SSI00_B/ SCK11_B/ SCL11_B	—	—	—
15	10	9	7	—	P200	IRQ0_A/NMI	—	—	—	—	—	—
16	11	10	8	SWCLK	P300	—	Ti04_B/TO04_B	—	—	—	—	—
17	12	11	9	SWDIO	P108	—	Ti03_B/TO03_B	—	—	—	—	—
18	13	12	—	—	P109	IRQ4_B	Ti02_A/TO02_A	—	TXD2_A/ SO20_A	SDAA0_C	TXDA0_C	—
19	14	13	—	—	P110	IRQ3_B	Ti01_A/TO01_A	—	RXD2_A/ SI20_A/ SDA20_A	SCLA0_C	RXDA0_C	—
20	15	14	—	—	P112	IRQ2_B	Ti03_A/TO03_A	—	SCK20_A/ SCL20_A/ SSI00_C	—	—	—
21	—	—	—	—	P103	IRQ5_A	Ti05_A/TO05_A	—	SSI00_A	—	—	—
22	16	15	10	PCLBUZ0_B	P102	IRQ4_A	Ti06_A/ TO06_A/ TO00_C	RTCCOUT_C	SCK00_A/ SCL00_A	—	—	—
23	17	16	11	—	P101	IRQ3_A	Ti07_A/ TO07_A/Ti00_C	—	TXD0_A/ SO00_A	SDAA0_D	TXDA0_D	AN021
24	18	17	12	—	P100	IRQ2_A	Ti04_A/ TO04_A/ Ti01_B/TO01_B	—	RXD0_A/ SI00_A/ SDA00_A	SCLA0_D	RXDA0_D	AN022
25	19	—	—	—	P015	IRQ1_A	—	—	—	—	—	AN007
26	20	—	—	—	P014	—	—	—	—	—	—	AN006
27	21	18	—	—	P013	—	—	—	—	—	—	AN005
28	22	19	13	—	P012	—	—	—	—	—	—	AN004
29	—	—	—	—	P009	—	—	—	—	—	—	AN003
30	—	—	—	—	P008	—	—	—	—	—	—	AN002
31	23	20	14	VREFL0	P011	—	—	—	—	—	—	AN001
32	24	1	15	VREFH0	P010	—	—	—	—	—	—	AN000

Note 1. When setting CMC.XTSEL = 1 for 24-, 20-, and 16-pin products

Note: Some signal names have \_A, \_B, \_C or \_D suffixes, but these suffixes can be ignored when assigning functionality, except for SAU and IICA. For SAU and IICA, only signals, except for SCK11, SCL11, and SSI00, bearing the same suffix can be selected. Assigning the same function to two or more pins simultaneously is prohibited.

[After correction of Table 1.15 Pin list] (UM P38)

Pin number				Power, System, Clock, Debug	I/O ports	Interrupt	Timers		Communication interfaces			Analogs
32-pin	24-pin	20-pin	16-pin				TAU	RTC	SAU	IICA	UARTA	ADC
1	1	2	16	VCL	—	—	—	—	—	—	—	—
2	—	—	—	XCIN	P215	—	—	—	—	—	—	—
3	—	—	—	XCOUT	P214	—	—	—	—	—	—	—
4	2	3	1	VSS	—	—	—	—	—	—	—	—
5	3	4	2	X2/EXCLK/ XCOUT <sup>*1</sup>	P213	IRQ0_B	Ti00_A/Ti02_B/ TO02_B	—	TXD1_A/ SO11_A	SDAA0_B	TXDA0_B	—
6	4	5	3	X1/XCIN <sup>*1</sup>	P212	IRQ1_B	TO00_A/ Ti03_C/TO03_C	—	RXD1_A/ SI11_A/ SDA11_A	SCLA0_B	RXDA0_B	—
7	5	6	4	VCC	—	—	—	—	—	—	—	—
8	—	—	—	PCLBUZ0_C	P407	IRQ4_C	—	RTCCOUT_A	SCK11_A/ SCL11_A	—	—	—
9	6	—	—	—	P914	—	—	—	—	SCLA0_A	—	—
10	7	—	—	—	P913	—	—	—	—	SDAA0_A	—	—
11	—	—	—	—	P208	IRQ3_C	Ti00_B	—	—	—	TXDA0_A	—
12	—	—	—	—	P207	IRQ2_C	TO00_B	—	—	—	RXDA0_A	—
13	8	7	5	RES	P206	—	—	—	—	—	—	—
14	9	8	6	PCLBUZ0_A	P201	IRQ5_B	Ti05_B/TO05_B	RTCCOUT_B	SSI00_B/ SCK11_B/ SCL11_B	—	—	—
15	10	9	7	—	P200	IRQ0_A/NMI	—	—	—	—	—	—
16	11	10	8	SWCLK	P300	—	Ti04_B/TO04_B	—	—	—	—	—
17	12	11	9	SWDIO	P108	—	Ti03_B/TO03_B	—	—	—	—	—
18	13	12	—	—	P109	IRQ4_B	Ti02_A/TO02_A	—	TXD2_A/ SO20_A	SDAA0_C	TXDA0_C	—
19	14	13	—	—	P110	IRQ3_B	Ti01_A/TO01_A	—	RXD2_A/ SI20_A/ SDA20_A	SCLA0_C	RXDA0_C	—
20	15	14	—	—	P112	IRQ2_B	Ti03_A/TO03_A	—	SCK20_A/ SCL20_A/ SSI00_C	—	—	—
21	—	—	—	—	P103	IRQ5_A	Ti05_A/TO05_A	—	SSI00_A	—	—	—
22	16	15	10	PCLBUZ0_B	P102	IRQ4_A	Ti06_A/ TO06_A/ TO00_C	RTCCOUT_C	SCK00_A/ SCL00_A	—	—	—
23	17	16	11	—	P101	IRQ3_A	Ti07_A/ TO07_A/Ti00_C	—	TXD0_A/ SO00_A	SDAA0_D	TXDA0_D	AN021
24	18	17	12	—	P100	IRQ2_A	Ti04_A/ TO04_A/ Ti01_B/TO01_B	—	RXD0_A/ SI00_A/ SDA00_A	SCLA0_D	RXDA0_D	AN022
25	19	—	—	—	P015	IRQ1_A	—	—	—	—	—	AN007
26	20	—	—	—	P014	—	—	—	—	—	—	AN006
27	21	18	—	—	P013	—	—	—	—	—	—	AN005
28	22	19	13	—	P012	—	—	—	—	—	—	AN004
29	—	—	—	—	P009	—	—	—	—	—	—	AN003
30	—	—	—	—	P008	—	—	—	—	—	—	AN002
31	23	20	14	VREFL0	P011	—	—	—	—	—	—	AN001
32	24	1	15	VREFH0	P010	—	—	—	—	—	—	AN000

Note 1. When setting CMC.XTSEL = 1 for 24-, 20-, and 16-pin products

**XCOUT and XCIN are not available on the 20-pin TSSOP product.**

Note: Some signal names have \_A, \_B, \_C or \_D suffixes, but these suffixes can be ignored when assigning functionality, except for SAU and IICA. For SAU and IICA, only signals, except for SCK11, SCL11, and SSI00, bearing the same suffix can be selected. Assigning the same function to two or more pins simultaneously is prohibited.

[Before correction of Figure 8.2 Clock generation circuit block diagram (24-, 20-, 16-pin) and Table 8.3 Clock generation circuit input/output pins] (UM P76)

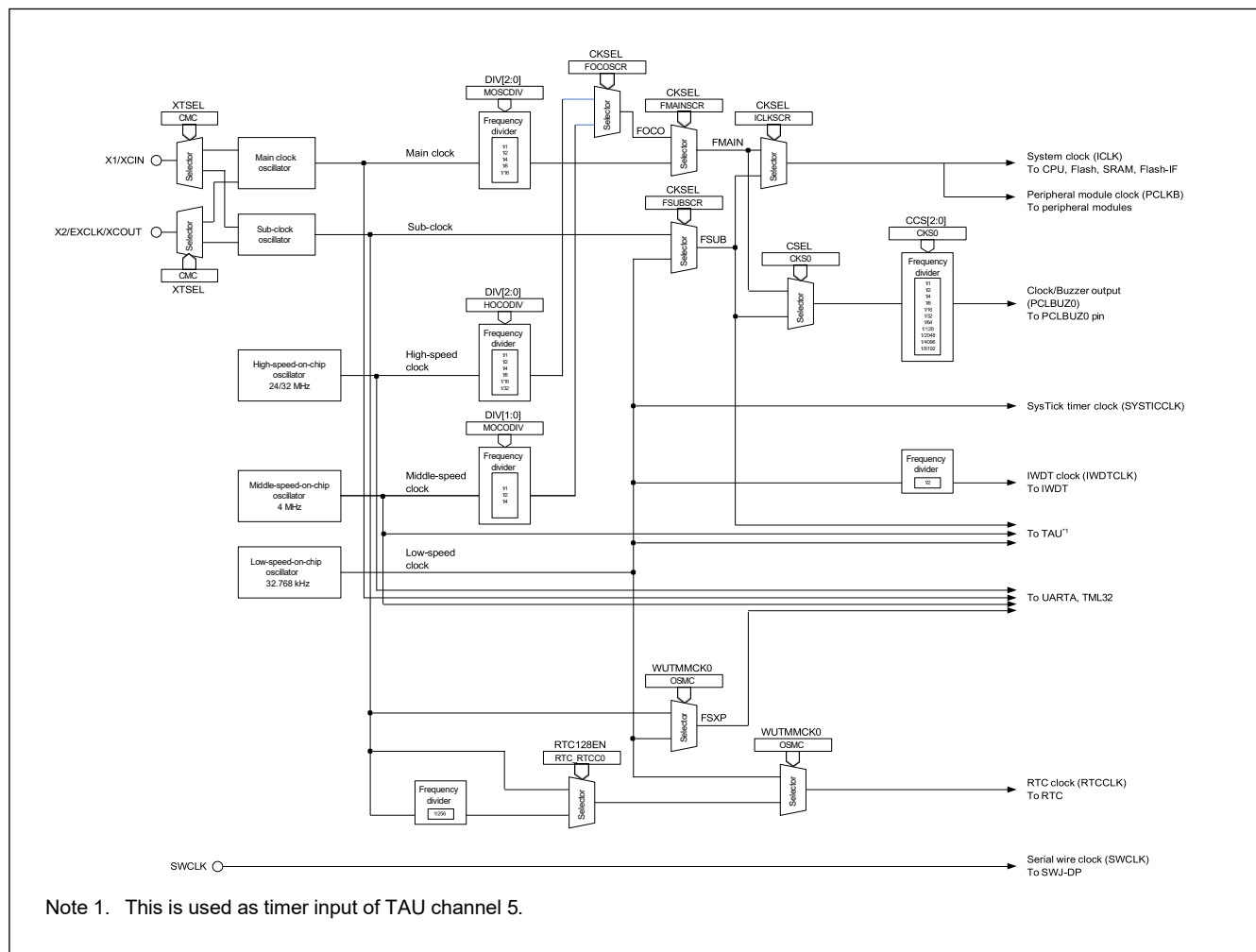
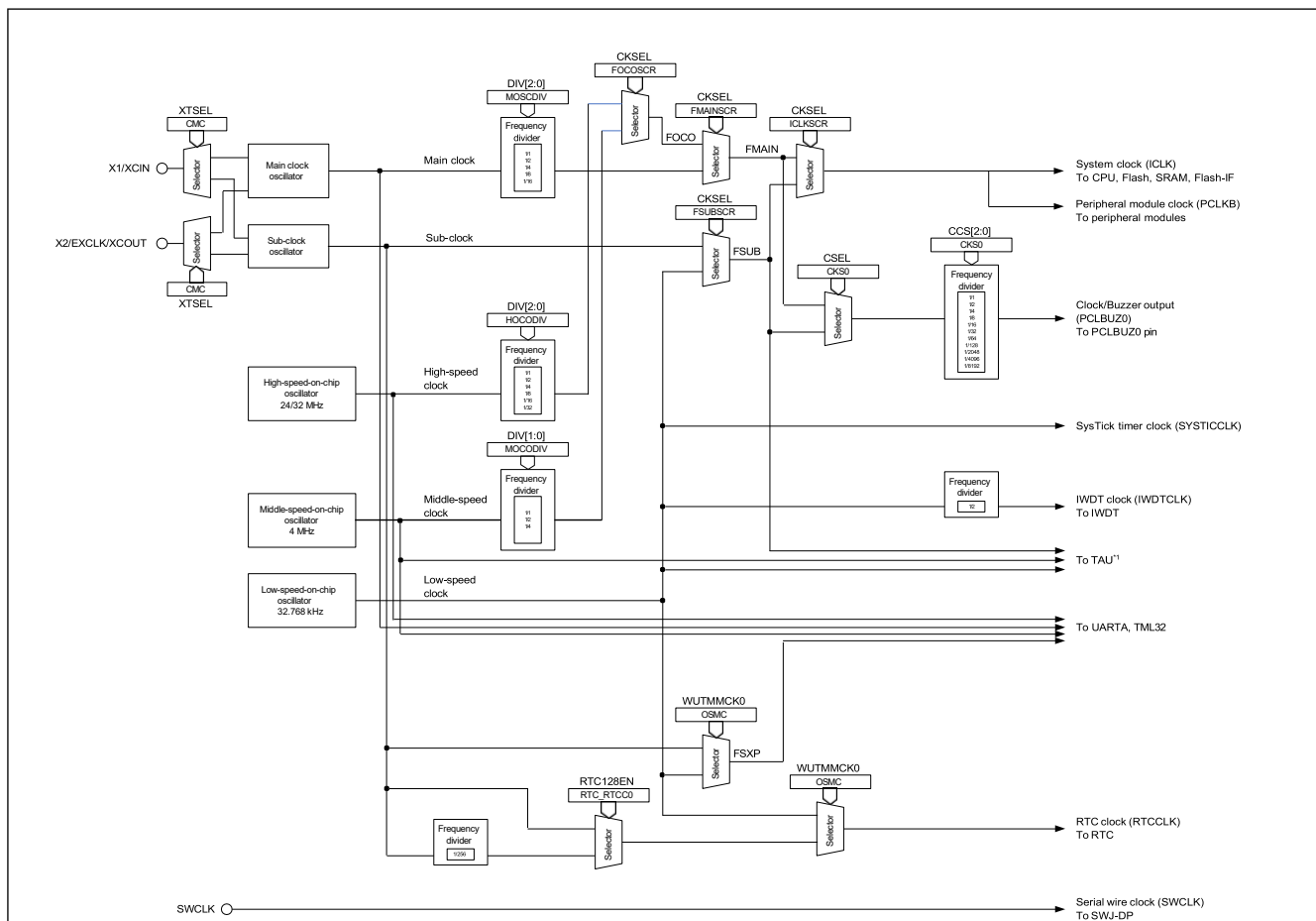


Figure 8.2 Clock generation circuit block diagram (24-, 20-, 16-pin)

Table 8.3 Clock generation circuit input/output pins

Pin name	I/O	Description
X1	Output	These pins are used to connect a crystal resonator. The EXCLK pin can also be used to input an external clock. For details, see <a href="#">section 8.3.2. External Clock Input</a> .
X2/EXCLK	Input	
XCIN	Input	These pins are used to connect a 32.768-kHz crystal resonator
XCOUT	Output	
PCLBUZ0	Output	This pin is used to output the CLKOUT/BUZZER clock
SWCLK	Input	This pin is used to input from the SWD

[After correction of Figure 8.2 Clock generation circuit block diagram (24-, 20-, 16-pin) and Table 8.3 Clock generation circuit input/output pins] (UM P76)



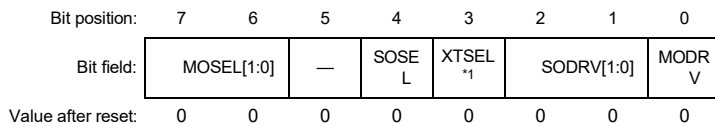
Note. The sub clock oscillator and its pins (XCOUT and XCIN) are not available on the 20 pin TSSOP package.  
 Note 1. This is used as timer input of TAU channel 5.

Figure 8.2 Clock generation circuit block diagram (24-, 20-, 16-pin)

Table 8.3 Clock generation circuit input/output pins

Pin name	I/O	Description
X1	Output	These pins are used to connect a crystal resonator. The EXCLK pin can also be used to input an external clock. For details, see <a href="#">section 8.3.2. External Clock Input</a> .
X2/EXCLK	Input	
XCIN	Input	These pins are used to connect a 32.768-kHz crystal resonator <b>Not available on the 20-pin TSSOP product.</b>
XCOUT	Output	
PCLBUZ0	Output	This pin is used to output the CLKOUT/BUZZER clock
SWCLK	Input	This pin is used to input from the SWD

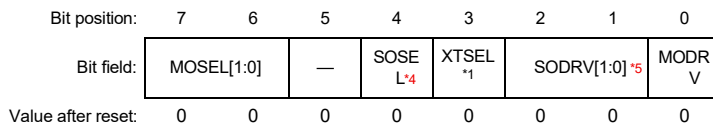
**[Before correction of 8.2.1 CMC : Clock Operation Mode Control Register] (UM P76,77)**



Bit	Symbol	Function	R/W
0	MODRV	Main Clock Oscillator Drive Capability Switching 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz	R/W
2:1	SODRV[1:0]	Sub-clock Oscillator Drive Capability Switching 0 0: Low Power Mode 1 0 1: Normal Mode 1 0: Low Power Mode 2 1 1: Low Power Mode 3	R/W
3	XTSEL	Selecting Clock Oscillator 0: Select MOSEL Contents <sup>*2</sup> 1: Select SOSEL Contents	R/W <sup>*3</sup>
4	SOSEL	Sub-clock Oscillator Switching 0: Port mode 1: Resonator	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
7:6	MOSEL[1:0]	Main Clock Oscillator Switching 0 1: Resonator 1 1: External clock input mode Others: Port mode	R/W

- Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
- Note: The CMC register can be written only once after release from the reset state.
- Note 1. The setting is fixed to "0" for products with 32 pins.
- Note 2. Using the main clock oscillator as a clock source in Low-speed mode is prohibited.
- Note 3. "R/W" for products with 24 pins or fewer, "R" only for products with 32 pins.

[After correction of 8.2.1 CMC : Clock Operation Mode Control Register] (UM P76,77)



Bit	Symbol	Function	R/W
0	MODRV	Main Clock Oscillator Drive Capability Switching 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz	R/W
2:1	SODRV[1:0]	Sub-clock Oscillator Drive Capability Switching 0 0: Low Power Mode 1 0 1: Normal Mode 1 0: Low Power Mode 2 1 1: Low Power Mode 3	R/W
3	XTSEL	Selecting Clock Oscillator 0: Select MOSEL Contents <sup>*2</sup> 1: Select SOSEL Contents	R/W <sup>*3</sup>
4	SOSEL	Sub-clock Oscillator Switching 0: Port mode 1: Resonator	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
7:6	MOSEL[1:0]	Main Clock Oscillator Switching 0 1: Resonator 1 1: External clock input mode Others: Port mode	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: The CMC register can be written only once after release from the reset state.

Note 1. The setting is fixed to "0" for products with 32 pins.

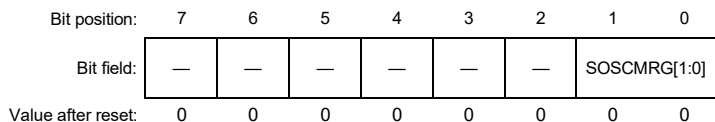
Note 2. Using the main clock oscillator as a clock source in Low-speed mode is prohibited.

Note 3. "R/W" for products with 24 pins or fewer, "R" only for products with 32 pins.

Note 4. For the 20-pin TSSOP product, set this bit to 0.

Note 5. For the 20-pin TSSOP product, set these bits to 00b.

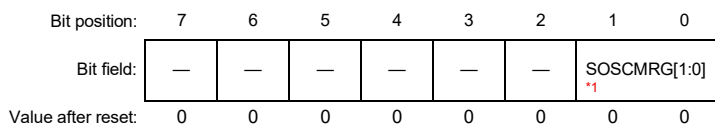
**[Before correction of 8.2.2 SOMRG : Sub-clock Oscillator Margin Check Register] (UM P78)**



Bit	Symbol	Function	R/W
1:0	SOSCMRG[1:0]	Sub-clock Oscillator Margin Check Switching 0 0: Normal Current 0 1: Lower Margin check 1 0: Upper Margin check 1 1: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

**[After correction of 8.2.2 SOMRG : Sub-clock Oscillator Margin Check Register] (UM P78)**

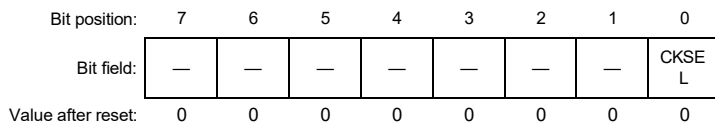


Bit	Symbol	Function	R/W
1:0	SOSCMRG[1:0]	Sub-clock Oscillator Margin Check Switching 0 0: Normal Current 0 1: Lower Margin check 1 0: Upper Margin check 1 1: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note1: For the 20-pin TSSOP product, set these bits to 00b.

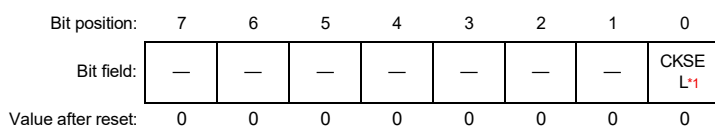
**[Before correction of 8.2.5 FSUBSCR : FSUB Clock Source Control Register] (UM P79)**



Bit	Symbol	Function	R/W
0	CKSEL	FSUB Clock Source Select 0: SOSC 1: LOCO	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

**[After correction of 8.2.5 FSUBSCR : FSUB Clock Source Control Register] (UM P79)**

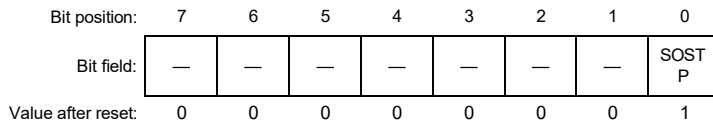


Bit	Symbol	Function	R/W
0	CKSEL	FSUB Clock Source Select 0: SOSC 1: LOCO	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

**Note1:** For the 20-pin TSSOP product, when using the subsystem clock (FSUB), select LOCO by setting the CKSEL bit to 1.

**[Before correction of 8.2.8 SOSCCR : Sub-clock Oscillator Control Register] (UM P81)**



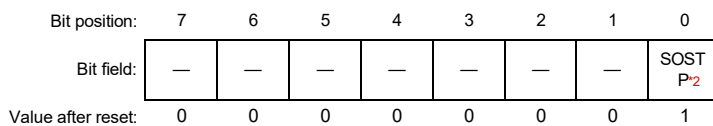
Bit	Symbol	Function	R/W
0	SOSTP	Sub-clock Oscillator Stop 0: Operate the sub-clock oscillator*1 1: Stop the sub-clock oscillator	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. The CMC register must be set before setting SOSTP to 0.

The SOSCCR register controls the sub-clock oscillator.

**[After correction of 8.2.8 SOSCCR : Sub-clock Oscillator Control Register] (UM P81)**



Bit	Symbol	Function	R/W
0	SOSTP	Sub-clock Oscillator Stop 0: Operate the sub-clock oscillator*1 1: Stop the sub-clock oscillator	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

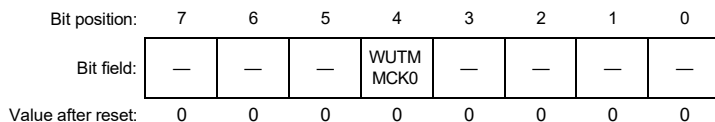
Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. The CMC register must be set before setting SOSTP to 0.

Note 2. For the 20-pin TSSOP product, set this bit to 1.

The SOSCCR register controls the sub-clock oscillator.

**[Before correction of 8.2.18 OSMC : Subsystem Clock Supply Mode Control Register] (UM P89)**



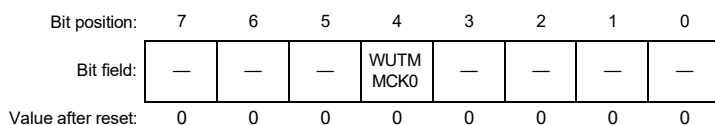
Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	WUTMMCK0	Selection of the Operating clock source for the Realtime Clock, 32-bit Interval Timer, Serial Interface UARTA 0: SOSC 1: LOCO*1 *2	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. After stopping SOSC, the clock source can be changed from SOSC to LOCO.

Note 2. Switching between SOSC and LOCO clock can be enabled by the WUTMMCK0 bit only when all of the realtime clock, 32-bit interval timer, and serial interface UARTA are stopped.

**[After correction of 8.2.18 OSMC : Subsystem Clock Supply Mode Control Register] (UM P89)**



Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	WUTMMCK0*3	Selection of the Operating clock source for the Realtime Clock, 32-bit Interval Timer, Serial Interface UARTA 0: SOSC 1: LOCO*1 *2	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. After stopping SOSC, the clock source can be changed from SOSC to LOCO.

Note 2. Switching between SOSC and LOCO clock can be enabled by the WUTMMCK0 bit only when all of the realtime clock, 32-bit interval timer, and serial interface UARTA are stopped.

Note 3. For the 20-pin TSSOP product, SOSC is not available. When supplying the subsystem clock as the operating clock source for the real-time clock, 32-bit interval timer, or UARTA serial interface, select LOCO by setting the WUTMMCK0 bit to 1.

**[Before correction of 8.4 Sub-clock Oscillator] (UM P93)**

The only way of supplying a clock signal to the sub-clock oscillator is by connecting a crystal oscillator.

**[After correction of 8.4 Sub-clock Oscillator] (UM P93)**

The only way of supplying a clock signal to the sub-clock oscillator is by connecting a crystal oscillator.

Note: The sub-clock oscillator is not available on the 20-pin TSSOP product.

**[Before correction of Table 18.1 Specifications of 32-bit interval timer operations] (UM P285)**

Item	Description
Count source (operating clock)	<ul style="list-style-type: none"> <li>• HOCO</li> <li>• MOCO</li> <li>• MOSC</li> <li>• LOCO/SOSC (LOCO or SOSC)*1</li> <li>• Event input from the ELC</li> </ul>
Capture clock (Selectable sources for counting by the timer which can generate a capture trigger)	<ul style="list-style-type: none"> <li>• HOCO</li> <li>• MOCO</li> <li>• MOSC</li> <li>• LOCO/SOSC (LOCO or SOSC)*1</li> <li>• Event input from the ELC</li> </ul>
Frequency division ratio	<ul style="list-style-type: none"> <li>• 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128</li> </ul>
Operating mode	<ul style="list-style-type: none"> <li>• 8-bit counter mode Channels 0 to 3 independently operate as 8-bit counters.</li> <li>• 16-bit counter mode The combinations of channels 0 and 1 and channels 2 and 3 are cascade-connectable to operate as two 16-bit counters.</li> <li>• 32-bit counter mode Channels 0 to 3 are connected to operate as a 32-bit counter.</li> <li>• 16-bit capture mode Channels 0 and 1 are connected to operate as a 16-bit counter using the count source, channels 2 and 3 are connected to operate as a 16-bit counter using the capture clock, and the connected counters are used for capture operation.</li> </ul>
Interrupt	<ul style="list-style-type: none"> <li>• Five interrupt sources are integrated into one interrupt signal and output as the TML32_ITL_OR signal.                             <ul style="list-style-type: none"> <li>– Output when the counter value in any of channels 0 to 3 matches the compare value.</li> <li>– Output when the capturing of the counter value is completed in capture mode.</li> </ul> </li> </ul>
Event link function	<ul style="list-style-type: none"> <li>• Four trigger signals TML32_ITL0 to TML32_ITL3 for the ELC are output.                             <ul style="list-style-type: none"> <li>– Output when the counter value in any of channels 0 to 3 matches the compare value.</li> </ul> </li> </ul>

Note 1. Select either LOCO or SOSC as the FSXP by setting the OSMC.WUTMMCK0 bit.

[After correction of Table 18.1 Specifications of 32-bit interval timer operations] (UM P285)

Item	Description
Count source (operating clock)	<ul style="list-style-type: none"> <li>• HOCO</li> <li>• MOCO</li> <li>• MOSC</li> <li>• LOCO/SOSC (LOCO or SOSC)*1</li> <li>• Event input from the ELC</li> </ul>
Capture clock (Selectable sources for counting by the timer which can generate a capture trigger)	<ul style="list-style-type: none"> <li>• HOCO</li> <li>• MOCO</li> <li>• MOSC</li> <li>• LOCO/SOSC (LOCO or SOSC)*1</li> <li>• Event input from the ELC</li> </ul>
Frequency division ratio	<ul style="list-style-type: none"> <li>• 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128</li> </ul>
Operating mode	<ul style="list-style-type: none"> <li>• 8-bit counter mode Channels 0 to 3 independently operate as 8-bit counters.</li> <li>• 16-bit counter mode The combinations of channels 0 and 1 and channels 2 and 3 are cascade-connectable to operate as two 16-bit counters.</li> <li>• 32-bit counter mode Channels 0 to 3 are connected to operate as a 32-bit counter.</li> <li>• 16-bit capture mode Channels 0 and 1 are connected to operate as a 16-bit counter using the count source, channels 2 and 3 are connected to operate as a 16-bit counter using the capture clock, and the connected counters are used for capture operation.</li> </ul>
Interrupt	<ul style="list-style-type: none"> <li>• Five interrupt sources are integrated into one interrupt signal and output as the TML32_ITL_OR signal.                         <ul style="list-style-type: none"> <li>– Output when the counter value in any of channels 0 to 3 matches the compare value.</li> <li>– Output when the capturing of the counter value is completed in capture mode.</li> </ul> </li> </ul>
Event link function	<ul style="list-style-type: none"> <li>• Four trigger signals TML32_ITL0 to TML32_ITL3 for the ELC are output.                         <ul style="list-style-type: none"> <li>– Output when the counter value in any of channels 0 to 3 matches the compare value.</li> </ul> </li> </ul>

Note 1. Select either LOCO or SOSC as the FSXP by setting the OSMC.WUTMMCK0 bit.

For the 20-pin TSSOP product, SOSC is not available.

**[Before correction of Table 19.1 RTC specifications] (UM P302)**

Item	Description
Count mode	Calendar count mode
Count source	<ul style="list-style-type: none"> <li>• Sub-clock (SOSC) or LOCO</li> <li>• 128-Hz from sub-clock (SOSC/256)</li> </ul>
Calendar functions	Year, month, date, day of week, hour, minute, and second are counted for up to 99 years
Interrupts (RTC_ALM_OR_PRD)	The following two interrupts are the source of the realtime clock interrupt signal (RTC_ALM_OR_PRD). <ul style="list-style-type: none"> <li>• Fixed-cycle interrupt                             <ul style="list-style-type: none"> <li>– Period selectable from among 0.5 of a second, 1 second, 1 minute, 1 hour, 1 day, or 1 month</li> </ul> </li> <li>• Alarm interrupt                             <ul style="list-style-type: none"> <li>– Alarm set by day of week, hour, and minute</li> </ul> </li> </ul>
Pin output function	1 Hz clock output

The realtime clock interrupt signal (RTC\_ALM\_OR\_PRD) can be used to wake up the MCU from the Software Standby mode or to trigger transitions to the Snooze mode.

**[After correction of Table 19.1 RTC specifications] (UM P302)**

Item	Description
Count mode	Calendar count mode
Count source*	<ul style="list-style-type: none"> <li>• Sub-clock (SOSC) or LOCO</li> <li>• 128-Hz from sub-clock (SOSC/256)</li> </ul>
Calendar functions	Year, month, date, day of week, hour, minute, and second are counted for up to 99 years
Interrupts (RTC_ALM_OR_PRD)	The following two interrupts are the source of the realtime clock interrupt signal (RTC_ALM_OR_PRD). <ul style="list-style-type: none"> <li>• Fixed-cycle interrupt                             <ul style="list-style-type: none"> <li>– Period selectable from among 0.5 of a second, 1 second, 1 minute, 1 hour, 1 day, or 1 month</li> </ul> </li> <li>• Alarm interrupt                             <ul style="list-style-type: none"> <li>– Alarm set by day of week, hour, and minute</li> </ul> </li> </ul>
Pin output function	1 Hz clock output

The realtime clock interrupt signal (RTC\_ALM\_OR\_PRD) can be used to wake up the MCU from the Software Standby mode or to trigger transitions to the Snooze mode.

**Note:** SOSC is not available as the count source for the 20-pin TSSOP product.

**[Before correction of Table 23.1 UARTA specifications] (UM P526)**

Item	Specifications
Serial interface modes	<ul style="list-style-type: none"> <li>• Operation stop mode</li> <li>• UART mode</li> </ul>
Interfaces	<ul style="list-style-type: none"> <li>• TXDA0: Transmit data output pin</li> <li>• RXDA0: Receive data input pin</li> </ul>
Operation clock sources	Operating clock independent of the CPU/peripheral hardware clock selectable to MOSC, HOCO, MOCO and FSXP (LOCO or SOSC)* <sup>1</sup>
Transfer rate	Up to 153.6 kbps
Baud rate	Settable with the dedicated internal 8-bit baud rate generator
Data format	<ul style="list-style-type: none"> <li>• MSB-first or LSB-first selectable</li> <li>• Transfer bit length selectable to 5, 7, or 8 bits</li> </ul>
Interrupt sources (UARTA0_TXI/UARTA0_RXI/UARTA0_ERRI)	<ul style="list-style-type: none"> <li>• Transfer completion interrupt</li> <li>• Reception transfer end</li> <li>• Reception error interrupt</li> </ul>
Other functions	<ul style="list-style-type: none"> <li>• Transmission and reception independent of each other (full-duplex communication)</li> <li>• Inversion control of communication logic level provided</li> <li>• Loopback mode</li> </ul>
Module-stop function	Module-stop state can be set to reduce power consumption

Note 1. Selectable either LOCO or SOSC as the FSXP by setting the OSMC\_WUTMMCK0 bit.

**[After correction of Table 23.1 UARTA specifications] (UM P526)**

Item	Specifications
Serial interface modes	<ul style="list-style-type: none"> <li>• Operation stop mode</li> <li>• UART mode</li> </ul>
Interfaces	<ul style="list-style-type: none"> <li>• TXDA0: Transmit data output pin</li> <li>• RXDA0: Receive data input pin</li> </ul>
Operation clock sources	Operating clock independent of the CPU/peripheral hardware clock selectable to MOSC, HOCO, MOCO and FSXP (LOCO or SOSC)* <sup>1*2</sup>
Transfer rate	Up to 153.6 kbps
Baud rate	Settable with the dedicated internal 8-bit baud rate generator
Data format	<ul style="list-style-type: none"> <li>• MSB-first or LSB-first selectable</li> <li>• Transfer bit length selectable to 5, 7, or 8 bits</li> </ul>
Interrupt sources (UARTA0_TXI/UARTA0_RXI/UARTA0_ERRI)	<ul style="list-style-type: none"> <li>• Transfer completion interrupt</li> <li>• Reception transfer end</li> <li>• Reception error interrupt</li> </ul>
Other functions	<ul style="list-style-type: none"> <li>• Transmission and reception independent of each other (full-duplex communication)</li> <li>• Inversion control of communication logic level provided</li> <li>• Loopback mode</li> </ul>
Module-stop function	Module-stop state can be set to reduce power consumption

Note 1. Selectable either LOCO or SOSC as the FSXP by setting the OSMC\_WUTMMCK0 bit.

Note 2. For the 20-pin TSSOP product, SOSC is not available as an operating clock source.

**[Before correction of Table 25.1 ADC12 specifications (2 of 2)] (UM P556)**

Parameter	Specifications
Reference voltage	<ul style="list-style-type: none"> <li>• VREFH0, VCC, or internal reference voltage (BGR) (external reference voltage or output voltage from reference voltage generation circuit) can be selected as the analog reference voltage.</li> <li>• VREFL0 or VSS can be selected as the analog reference ground.</li> </ul>
Module-stop function	Module-stop state can be set to reduce power consumption.*2

Note 1. AN000 to AN007, AN021, AN022 for LQFP/HWQFN 32-pin  
 AN000, AN001, AN004 to AN007, AN021, AN022 for HWQFN 24-pin  
 AN000, AN001, AN004, AN005, AN021. AN022 for LSSOP 20-pin  
 AN000, AN001, AN004, AN021. AN022 for HWQFN 16-pin

Note 2. For details, see [section 9, Low Power Modes](#).

**[After correction of Table 25.1 ADC12 specifications (2 of 2)] (UM P556)**

Parameter	Specifications
Reference voltage	<ul style="list-style-type: none"> <li>• VREFH0, VCC, or internal reference voltage (BGR) (external reference voltage or output voltage from reference voltage generation circuit) can be selected as the analog reference voltage.</li> <li>• VREFL0 or VSS can be selected as the analog reference ground.</li> </ul>
Module-stop function	Module-stop state can be set to reduce power consumption.*2

Note 1. AN000 to AN007, AN021, AN022 for LQFP/HWQFN 32-pin  
 AN000, AN001, AN004 to AN007, AN021, AN022 for HWQFN 24-pin  
 AN000, AN001, AN004, AN005, AN021. AN022 for LSSOP/TSSOP 20-pin  
 AN000, AN001, AN004, AN021. AN022 for HWQFN 16-pin

Note 2. For details, see [section 9, Low Power Modes](#).

**[Before correction of 31.2.2 Sub-clock Oscillator Characteristics] (UM P665)**

Conditions: VCC = 2.4 to 5.5 V (16- to 24-pin products), VCC = 1.6 to 5.5 V (32-pin products), VSS = 0 V, Ta = -40 to +105°C

Parameter		Min	Typ	Max	Unit	Test conditions
Sub-clock oscillation frequency (fsosc) <sup>*1</sup>	Crystal resonator	—	32.768	—	kHz	—

Note 1. The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

**[After correction of 31.2.2 Sub-clock Oscillator Characteristics] (UM P665)**

Conditions: VCC = 2.4 to 5.5 V (16- to 24-pin products), VCC = 1.6 to 5.5 V (32-pin products), VSS = 0 V, Ta = -40 to +105°C

Parameter		Min	Typ	Max	Unit	Test conditions
Sub-clock oscillation frequency (fsosc) <sup>*1</sup>	Crystal resonator	—	32.768	—	kHz	—

Note 1. The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

Note: This characteristic is not applicable to the 20-pin TSSOP.

[Before correction of Table 31.40 A/D conversion characteristics in Normal modes 1 and 2] (UM P709)

Table 31.40 A/D conversion characteristics in Normal modes 1 and 2 (2 of 2)

Conditions:  $2.4V \leq VREFH0 \leq VCC \leq 5.5 V$ ,  $VSS = 0 V$ ,  $Ta = -40$  to  $+105^{\circ}C$

Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).

Target pins: AN000 to AN007, AN021 to AN022, internal reference voltage, and temperature sensor output voltage

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Overall error*1 *3 *4 *5	12-bit resolution	AINL	—	—	±7.5	LSB	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±9.0	LSB	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±9.0	LSB	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Conversion time*6	12-bit resolution	t <sub>CONV</sub>	2.0	—	—	μs	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			2.0	—	—	μs	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			2.0	—	—	μs	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Zero-scale error*1 *2 *3 *4 *5	12-bit resolution	E <sub>ZS</sub>	—	—	±0.17	%FSR	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±0.21	%FSR	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±0.21	%FSR	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Full-scale error*1 *2 *3 *4 *5	12-bit resolution	E <sub>FS</sub>	—	—	±0.17	%FSR	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±0.21	%FSR	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±0.21	%FSR	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Integral linearity error*1 *4 *5	12-bit resolution	ILE	—	—	±3.0	LSB	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±3.0	LSB	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±3.0	LSB	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Differential linearity error*1	12-bit resolution	DLE	—	±1.0	—	LSB	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			—	±1.0	—	LSB	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			—	±1.0	—	LSB	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Analog input voltage	V <sub>AIN</sub>	0	—	VREFH0	V	—	

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When pins AN021 to AN022 are selected as the target pins for conversion, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Note 4. When reference voltage (+) = VCC (ADREFP[1:0] = 00b) and reference voltage (-) = VSS (ADREFM = 0b), the maximum values are as follows.

Overall error: Add ±10 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.

Integral linearity error: Add ±4 LSB to the maximum value.

Note 5. When VREFH0 < VCC, the maximum values are as follows.

Overall error / Zero-scale error / Full-scale error: Add ±0.75 LSB × (VCC - VREFH0) to the maximum value.

Integral linearity error: Add ±0.2 LSB × (VCC - VREFH0) to the maximum value.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 μs. Accordingly, use standard mode 2 with the longer sampling time.

[After correction of Table 31.40 A/D conversion characteristics in Normal modes 1 and 2] (UM P709)

Table 31.40 A/D conversion characteristics in Normal modes 1 and 2 (2 of 2)

Conditions:  $2.4V \leq VREFH0 \leq VCC \leq 5.5 V$ ,  $VSS = 0 V$ ,  $T_a = -40$  to  $+105^\circ C$

Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).

Target pins: AN000 to AN007, AN021 to AN022, internal reference voltage, and temperature sensor output voltage

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Overall error <sup>*1 *3 *4 *5 *7</sup>	12-bit resolution	AINL	—	—	±7.5	LSB	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±9.0	LSB	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±9.0	LSB	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Conversion time <sup>*6</sup>	12-bit resolution	t <sub>CONV</sub>	2.0	—	—	μs	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			2.0	—	—	μs	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			2.0	—	—	μs	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Zero-scale error <sup>*1 *2 *3 *4 *5 *7</sup>	12-bit resolution	E <sub>ZS</sub>	—	—	±0.17	%FSR	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±0.21	%FSR	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±0.21	%FSR	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Full-scale error <sup>*1 *2 *3 *4 *5 *7</sup>	12-bit resolution	E <sub>FS</sub>	—	—	±0.17	%FSR	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±0.21	%FSR	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±0.21	%FSR	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Integral linearity error <sup>*1 *4 *5 *7</sup>	12-bit resolution	ILE	—	—	±3.0	LSB	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±3.0	LSB	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			—	—	±3.0	LSB	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Differential linearity error <sup>*1 *7</sup>	12-bit resolution	DLE	—	±1.0	—	LSB	$4.5 V \leq VREFH0 = VCC \leq 5.5 V$
			—	±1.0	—	LSB	$2.7 V \leq VREFH0 = VCC \leq 5.5 V$
			—	±1.0	—	LSB	$2.4 V \leq VREFH0 = VCC \leq 5.5 V$
Analog input voltage	V <sub>AIN</sub>	0	—	VREFH0	V	—	

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When pins AN021 to AN022 are selected as the target pins for conversion, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Note 4. When reference voltage (+) = VCC (ADREFP[1:0] = 00b) and reference voltage (-) = VSS (ADREFM = 0b), the maximum values are as follows.

Overall error: Add ±10 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.

Integral linearity error: Add ±4 LSB to the maximum value.

Note 5. When VREFH0 < VCC, the maximum values are as follows.

Overall error / Zero-scale error / Full-scale error: Add ±0.75 LSB × (VCC - VREFH0) to the maximum value.

Integral linearity error: Add ±0.2 LSB × (VCC - VREFH0) to the maximum value.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 μs. Accordingly, use standard mode 2 with the longer sampling time.

Note 7. The values for the 20-pin TSSOP product are the results of characteristic evaluation and are not checked for shipment.

[Before correction of Table 31.41 A/D conversion characteristics in Low-voltage modes 1 and 2] (UM P709, 710)

Table 31.41 A/D conversion characteristics in Low-voltage modes 1 and 2 (1) (1 of 2)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).

Target pins: AN000 to AN007, AN021 to AN022, internal reference voltage\*7, and temperature sensor output voltage\*7

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Resolution	RES	8	—	12	bit	—	
Conversion clock	f <sub>AD</sub>	1	—	24	MHz	—	
Overall error*1 *3 *4 *5	12-bit resolution	AINL	—	—	±9	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±9	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±11.5	LSB	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±12.0	LSB	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V

Table 31.41 A/D conversion characteristics in Low-voltage modes 1 and 2 (1) (2 of 2)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).

Target pins: AN000 to AN007, AN021 to AN022, internal reference voltage\*7, and temperature sensor output voltage\*7

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Conversion time*6	12-bit resolution	t <sub>CONV</sub>	3.3	—	—	μs	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			5.0	—	—	μs	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			10.0	—	—	μs	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			20.0	—	—	μs	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Zero-scale error*1 *2 *3 *4 *5	12-bit resolution	E <sub>ZS</sub>	—	—	±0.21	%FSR	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.21	%FSR	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.27	%FSR	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.28	%FSR	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Full-scale error*1 *2 *3 *4 *5	12-bit resolution	E <sub>FS</sub>	—	—	±0.21	%FSR	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.21	%FSR	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.27	%FSR	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.28	%FSR	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Integral linearity error*1 *4 *5	12-bit resolution	ILE	—	—	±4.0	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±4.0	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±4.5	LSB	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±4.5	LSB	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Differential linearity error*1	12-bit resolution	DLE	—	±1.5	—	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±1.5	—	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±2.0	—	LSB	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±2.0	—	LSB	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Analog input voltage	V <sub>AIN</sub>	0	—	VREFH0	V	—	

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When pins AN021 to AN022 are selected as the target pins for conversion, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Note 4. When reference voltage (+) = VCC (ADREFP[1:0] = 00b) and reference voltage (-) = VSS (ADREFM = 0b), the maximum values are as follows.

Overall error: Add ±10 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.

Integral linearity error: Add ±4 LSB to the maximum value.

Note 5. When VREFH0 < VCC, the maximum values are as follows.

Overall error / Zero-scale error / Full-scale error: Add ±0.75 LSB × (VCC - VREFH0) to the maximum value.

Integral linearity error: Add ±0.2 LSB × (VCC - VREFH0) to the maximum value.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 μs. Accordingly, use standard mode 2 with the longer sampling time, and use the conversion clock (fAD) of no more than 16 MHz.

Note 7. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VCC must be at least 1.8 V.

**[After correction of Table 31.41 A/D conversion characteristics in Low-voltage modes 1 and 2] (UM P709, 710)**

Table 31.41 A/D conversion characteristics in Low-voltage modes 1 and 2 (1) (1 of 2)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).

Target pins: AN000 to AN007, AN021 to AN022, internal reference voltage\*7, and temperature sensor output voltage\*7

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		RES	8	—	12	bit	—
Conversion clock		fAD	1	—	24	MHz	—
Overall error*1 *3 *4 *5*8	12-bit resolution	AINL	—	—	±9	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±9	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±11.5	LSB	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±12.0	LSB	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V

Table 31.41 A/D conversion characteristics in Low-voltage modes 1 and 2 (1) (2 of 2)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).

Target pins: AN000 to AN007, AN021 to AN022, internal reference voltage\*7, and temperature sensor output voltage\*7

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Conversion time*6	12-bit resolution	tCONV	3.3	—	—	μs	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			5.0	—	—	μs	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			10.0	—	—	μs	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			20.0	—	—	μs	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Zero-scale error*1 *2 *3 *4 *5*8	12-bit resolution	EZS	—	—	±0.21	%FSR	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.21	%FSR	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.27	%FSR	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.28	%FSR	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Full-scale error*1 *2 *3 *4 *5*8	12-bit resolution	EFS	—	—	±0.21	%FSR	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.21	%FSR	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.27	%FSR	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.28	%FSR	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V

Integral linearity error*1 *4 *5*8	12-bit resolution	ILE	—	—	±4.0	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±4.0	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±4.5	LSB	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±4.5	LSB	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Differential linearity error*1*8	12-bit resolution	DLE	—	±1.5	—	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±1.5	—	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±2.0	—	LSB	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±2.0	—	LSB	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Analog input voltage		V <sub>AIN</sub>	0	—	VREFH0	V	—

Note 1. This value does not include the quantization error ( $\pm 1/2$  LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When pins AN021 to AN022 are selected as the target pins for conversion, the maximum values are as follows.

Overall error: Add  $\pm 3$  LSB to the maximum value.

Zero-scale/full-scale error: Add  $\pm 0.04\%$ FSR to the maximum value.

Note 4. When reference voltage (+) = VCC (ADREFP[1:0] = 00b) and reference voltage (-) = VSS (ADREFM = 0b), the maximum values are as follows.

Overall error: Add  $\pm 10$  LSB to the maximum value.

Zero-scale/full-scale error: Add  $\pm 0.25\%$ FSR to the maximum value.

Integral linearity error: Add  $\pm 4$  LSB to the maximum value.

Note 5. When VREFH0 < VCC, the maximum values are as follows.

Overall error / Zero-scale error / Full-scale error: Add  $\pm 0.75$  LSB  $\times$  (VCC - VREFH0) to the maximum value.

Integral linearity error: Add  $\pm 0.2$  LSB  $\times$  (VCC - VREFH0) to the maximum value.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5  $\mu$ s. Accordingly, use standard mode 2 with the longer sampling time, and use the conversion clock (f<sub>AD</sub>) of no more than 16 MHz.

Note 7. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VCC must be at least 1.8 V.

Note 8. The values for the 20-pin TSSOP product are the results of characteristic evaluation and are not checked for shipment.

**[Before correction of Table 31.42 A/D conversion characteristics in Low-voltage modes 1 and 2] (UM P710, 711)**

Table 31.42 A/D conversion characteristics in Low-voltage modes 1 and 2 (2) (1 of 2)

Conditions:  $1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ to }+105^\circ\text{C}$

Reference voltage range applied to the internal reference voltage (ADREFP[1:0] = 10b) and VREFL0 (ADREFM = 1b).

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution	RES	8			bit	—
Conversion clock	$f_{AD}$	1	—	2	MHz	$1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Zero-scale error <sup>*1 *2 *4</sup>	$E_{ZS}$	—	—	$\pm 0.6$	%FSR	$1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Integral linearity error <sup>*1 *4</sup>	ILE	—	—	$\pm 2.0$	LSB	$1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$

Table 31.42 A/D conversion characteristics in Low-voltage modes 1 and 2 (2) (2 of 2)

Conditions:  $1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ to }+105^\circ\text{C}$

Reference voltage range applied to the internal reference voltage (ADREFP[1:0] = 10b) and VREFL0 (ADREFM = 1b).

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Differential linearity error <sup>*1</sup>	DLE	—	$\pm 1.0$	—	LSB	$1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Analog input voltage	$V_{AIN}$	0	—	$V_{BGR}^{*3}$	V	—

Note 1. This value does not include the quantization error ( $\pm 1/2$  LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. Refer to [Table 31.44](#).

Note 4. When reference voltage (-) is selected as VSS, the maximum values are as follows.

Zero-scale error: Add  $\pm 0.35\%$ FSR to the maximum value.

Integral linearity error: Add  $\pm 0.5$  LSB to the maximum value.

[After correction of Table 31.42 A/D conversion characteristics in Low-voltage modes 1 and 2] (UM P710, 711)

Conditions:  $1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ to }+105^\circ\text{C}$

Reference voltage range applied to the internal reference voltage (ADREFP[1:0] = 10b) and VREFL0 (ADREFM = 1b).

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution	RES	8			bit	—
Conversion clock	$f_{AD}$	1	—	2	MHz	$1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Zero-scale error <sup>*1 *2 *4*5</sup>	$E_{ZS}$	—	—	$\pm 0.6$	%FSR	$1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Integral linearity error <sup>*1 *4*5</sup>	ILE	—	—	$\pm 2.0$	LSB	$1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$

Table 31.42 A/D conversion characteristics in Low-voltage modes 1 and 2 (2) (2 of 2)

Conditions:  $1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ to }+105^\circ\text{C}$

Reference voltage range applied to the internal reference voltage (ADREFP[1:0] = 10b) and VREFL0 (ADREFM = 1b).

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Differential linearity error <sup>*1*5</sup>	DLE	—	$\pm 1.0$	—	LSB	$1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Analog input voltage	$V_{AIN}$	0	—	$V_{BGR}^{*3}$	V	—

Note 1. This value does not include the quantization error ( $\pm 1/2$  LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. Refer to Table 31.44.

Note 4. When reference voltage (-) is selected as  $V_{SS}$ , the maximum values are as follows.

Zero-scale error: Add  $\pm 0.35\%$ FSR to the maximum value.

Integral linearity error: Add  $\pm 0.5$  LSB to the maximum value.

Note 5. The values for the 20-pin TSSOP product are the results of characteristic evaluation and are not checked for shipment.