

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0166A/E	Rev.	1.00
Title	RA8M1 Group, RA8D1 Group, RA8T1 Group, RA8E1 Group, and RA8E2 Group, correction of Pin list and function description		Information Category	Technical Notification		
Applicable Product	RA8M1 Group RA8D1 Group RA8T1 Group RA8E1 Group RA8E2 Group	Lot No.	Reference Document	RA8M1 Group User's Manual : Hardware Rev.1.20 RA8D1 Group User's Manual : Hardware Rev.1.20 RA8T1 Group User's Manual : Hardware Rev.1.20 RA8E1 Group User's Manual : Hardware Rev.1.10 RA8E2 Group User's Manual : Hardware Rev.1.10		
		All				

The contents of Pin list table, register settings for input/output pin function of PORT4 and Register settings for input/output pin function of PORT9 are corrected.

FSP (RA Flexible Software Package) has been correctly implemented. This is only User's Manual Hardware error.

1. **P403** function was shown as CTS_RTS4_A/SS4_A in SCI function in Pin List table and Port4 PSEL[4:0] register setting table.

These 2 tables are corrected as CTS_RTS1_A/SS1_A.

2. **Port9** PSEL[4:0] register setting for SCI function was shown as 00100b in Port4 register table.

This Table is corrected as 00101b.

3. Example of RA8M1 Group User's Manual: Hardware Rev.1.20 correction is as follows.

Correction in Table 1.16 Pin list (1 of 6)

Before correction

BGA 224	LQF P176	LQF P144	LQF P100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus, SDRAM	Ex. Interrupt	SCI/IIC/I3C/SPI/CANFD/USBF S/ USBHS/OSPI/SSIE/SDHI/MMC / EHTERC(MII,RMII)	GPT/AGT/ULP T/RTC	ADC12/ DAC12/ ACMPHS	CEU
N14	4	4	4	-	P403	-	IRQ14-DS	CTS_RTS4_A/SS4_A/DE1/ SSIBCK0_A/SD1DAT1_B/ ET0_LINKSTA/ET0_LINKSTA	GTIOC3A/RTCI- C1	-	-

After correction

BGA 224	LQF P176	LQF P144	LQF P100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus, SDRAM	Ex. Interrupt	SCI/IIC/I3C/SPI/CANFD/USBF S/ USBHS/OSPI/SSIE/SDHI/MMC / EHTERC(MII,RMII)	GPT/AGT/ULP T/RTC	ADC12/ DAC12/ ACMPHS	CEU
N14	4	4	4	-	P403	-	IRQ14-DS	CTS_RTS1_A/SS1_A/DE1/ SSIBCK0_A/SD1DAT1_B/ ET0_LINKSTA/ET0_LINKSTA	GTIOC3A/RTCI- C1	-	-

Correction in Table 19.10 Register settings for input/output pin function (PORT4)

Before correction

PSEL[4:0] settings	Function	Pin															
		P400	P401	P402	P403	P404	P405	P406	P407	P408	P409	P410	P411	P412	P413	P414	P415
00101b	SCI*2	TXD1_A/ MOSI1_A/ SDA1_A_C	RXD1_A/ MISO1_A/ SCL1_A	SCK1_A	CTS_R TS4_A SS4_A	CTS1_A	—	—	—	RXD3_A/ MISO3_A/ SCL3_A	TXD3_A/ MOSI3_A/ SDA3_A	SCK3_A	CTS_A RTS3_A SS3_A	CTS3_A	—	—	—

After correction

PSEL[4:0] settings	Function	Pin															
		P400	P401	P402	P403	P404	P405	P406	P407	P408	P409	P410	P411	P412	P413	P414	P415
00101b	SCI*2	TXD1_A/ MOSI1_A/ SDA1_A_C	RXD1_A/ MISO1_A/ SCL1_A	SCK1_A	CTS_R TS1_A SS1_A	CTS1_A	—	—	—	RXD3_A/ MISO3_A/ SCL3_A	TXD3_A/ MOSI3_A/ SDA3_A	SCK3_A	CTS_A RTS3_A SS3_A	CTS3_A	—	—	—

Correction in Table 19.15 Register settings for input/output pin function (PORT9)

Before correction

PSEL[4:0] settings	Function	Pin															
		P900	P901	P902	P903	P904	P905	P906	P907	P908	P909	P910	P911	P912	P913	P914	P915
00100b	SCI*1	TXD3_C/ MOSI3_C/ SDA3_C	RXD3_C/ MISO3_C/ SCL3_C	—	—	—	CTS3_B	—	—	—	—	—	—	—	—	—	—

After correction

PSEL[4:0] settings	Function	Pin															
		P900	P901	P902	P903	P904	P905	P906	P907	P908	P909	P910	P911	P912	P913	P914	P915
00101b	SCI*1	TXD3_C/ MOSI3_C/ SDA3_C	RXD3_C/ MISO3_C/ SCL3_C	—	—	—	CTS3_B	—	—	—	—	—	—	—	—	—	—

4. Affected tables in each Group User's Manual: Hardware.

User's Manual	Correction for P403 function from CTS_RTS4_A/SS4_A to CTS_RTS1_A/SS1_A		Correction for Port9 PSEL [4:0] register setting for SCI from 00100 b to 00101 b
	Pin list	Port4 PSEL [4:0] register setting	
RA8M1 Group User's Manual: Hardware Rev.1.20	Table 1.16 Pin list (1 of 6) Page (86/2725)	Table 19.10 Register settings for input/output pin function (PORT4) (2 of 2) Page (645/2725)	Table 19.15 Register settings for input/output pin function (PORT9) (1 of 2) Page (649/2725)
RA8D1 Group User's Manual: Hardware Rev.1.20	Table 1.16 Pin list (1 of 7) Page (94/3004)	Table 19.10 Register settings for input/output pin function (PORT4) (1 of 2) Page (674/3004)	Table 19.15 Register settings for input/output pin function (PORT9) (2 of 2) Page (679/3004)
RA8T1 Group User's Manual: Hardware Rev.1.20	Table 1.15 Pin list (1 of 6) Page (77/2325)	Table 18.9 Register settings for input/output pin function (PORT4) (2 of 2) Page (605/2325)	Table 18.14 Register settings for input/output pin function (PORT9) Page (609/2325)
RA8E1 Group User's Manual: Hardware Rev.1.10	Table 1.16 Pin list (1 of 4) Page (72/2095)	Table 19.10 Register settings for input/output pin function (PORT4) (1 of 2) Page (527/2095)	Table 19.15 Register settings for input/output pin function (PORT9) Page (531/2095)
RA8E2 Group User's Manual: Hardware Rev.1.10	Table 1.16 Pin list (1 of 5) Page (75/2219)	Table 19.10 Register settings for input/output pin function (PORT4) (1 of 2) Page (613/2219)	Table 19.15 Register settings for input/output pin function (PORT9) Page (617/2219)