Date: Jun. 16, 2025

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0113B/E	Rev.	2.00
Title	RZ/G1H, G1M, G1N and G1E Correction of section 15. External Bus Controller for DDR3-SDRAM (DBSC3)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, RZ/G1H, RZ/G1M, RZ/G1N, RZ/G1E	Lot No. All lots	Reference Document	RZ/G Series, User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100)		

This technical update describes document correction of RZ/G Series product.

[Summary]

Document correction for section 15. External Bus Controller for DDR3-SDRAM (DBSC3).

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G1H,

RZ/G1M,

RZ/G1N,

RZ/G1E

[Section number and title]

Section 15. External Bus Controller for DDR3-SDRAM (DBSC3)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 15.8 M0(/1) RESET# pin level during DDR power-up, new section is added.

Current (from):

— (none)

Correction (to):

RZ/G1H RZ/G1N
RZ/G1M RZ/G1E

15.9 M0(/1)RESET# pin level during DDR power-up

The pin level of M0(/1)RESET# is undefined during DDR power-up as shown in Figure 15.29

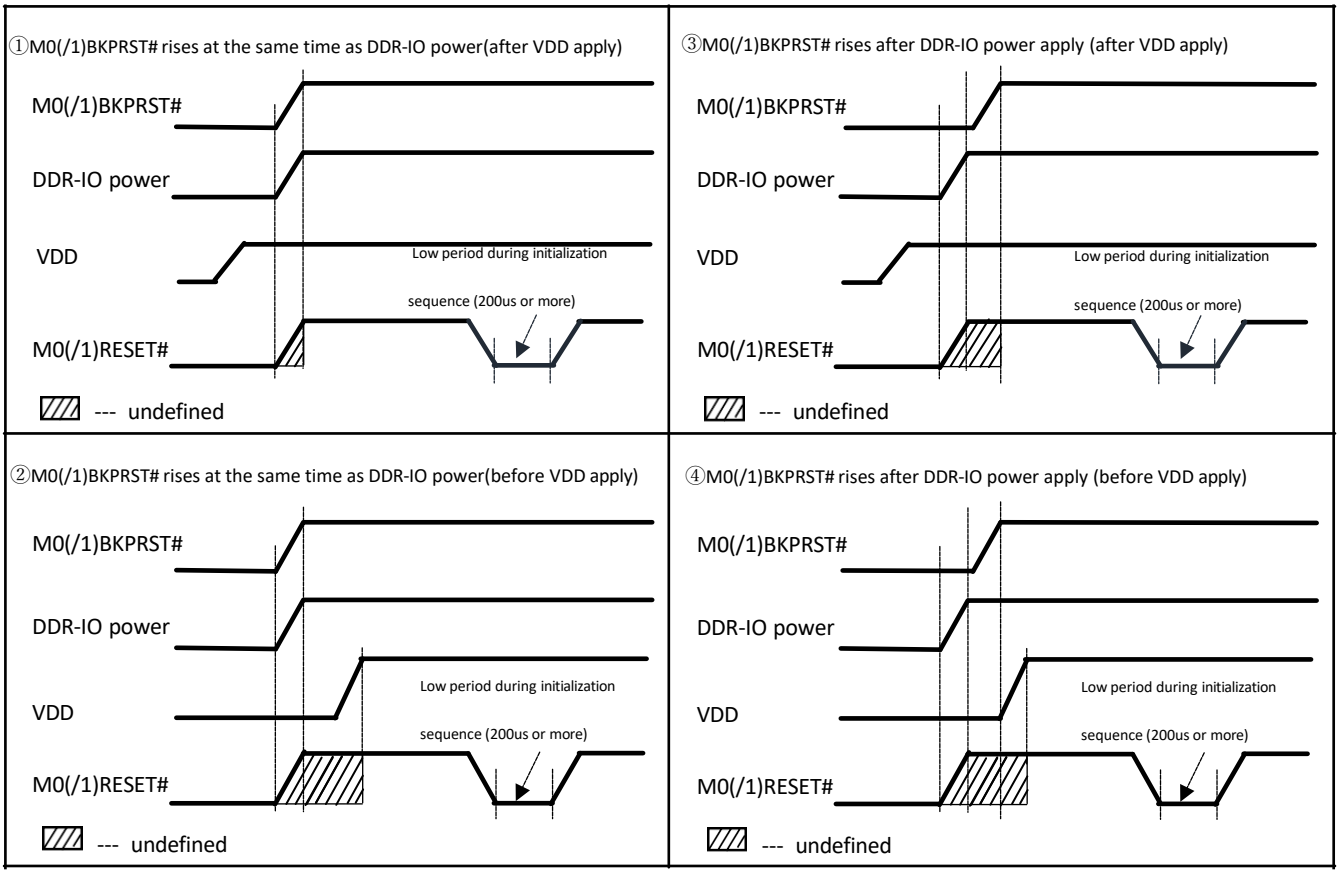


Figure 15.29 M0(/1)RESET# pin level during DDR power-up

[Description]

M0(/1)RESET# pin level during DDR power-up.

[Reason for Correction]

Caution for M0(/1)RESET# pin level during DDR power-up.

- End of Document –

Appendix

IMPLEMENTATION OF JEDEC STANDARD AND RENESAS RZ/G1x

In the JEDEC Standard (DDR3 SDRAM Standard JESD79-3E), the following chapter shows the regulations for reset.

3.3 RESET and Initialization Procedure

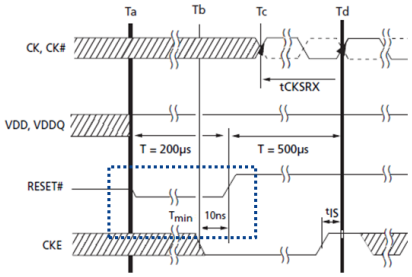
3.3.1 Power-up Initialization Sequence … Recommend "L" as default value of RESET ⇒ **Not supported in RZ/G1x**

3.3.2 Reset Initialization with Stable Power … Mandatory ⇒ **Supported in RZ/G1x**

3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.

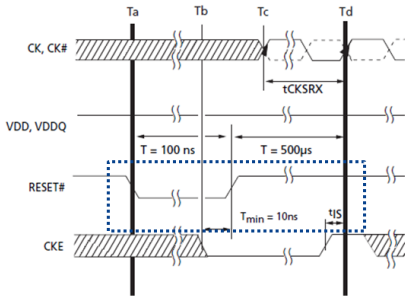


Reset and Initialization Sequence at Power-on Ramping

3.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2 * VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled "LOW" before RESET being de-asserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence steps 2 to 11.
3. The Reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



Reset Procedure at Power Stable Condition

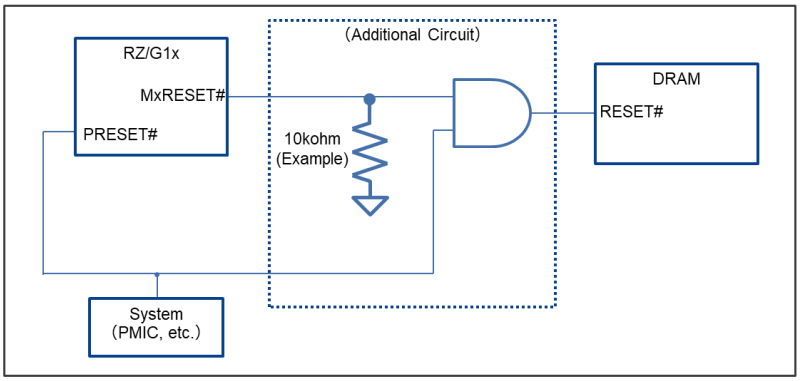
EXPECTED ISSUE AND COUNTERMEASURES

If RESET# is "H" at power-on, some DRAM products may not be initialized correctly.

In some DRAM products, initialization may not work as expected even if you try to initialize again with RESET# after the power has stabilized.

For this reason, with the RZ/G1x, it is necessary to add a circuit such as a pull-down resistor to set the initial state of the RESET# terminal to "L".

An example circuit is shown below.



External circuit notes:
The 10kohm pull-down resistor will increase the VDDQ_DDR current by up to 0.158mA (=1.575V(DDR3_max)/10kohm).

付録

JEDEC STANDARDと弊社RZ/G1x製品の実装に関して

JEDEC Standard (DDR3 SDRAM Standard JESD79-3E) では、以下の章にリセットの規定があります。

3.3 RESET and Initialization Procedure

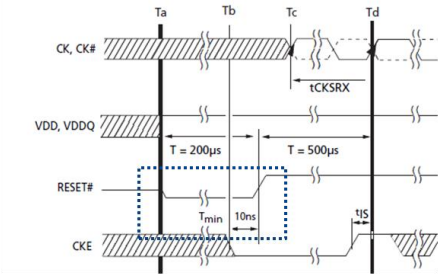
3.3.1 Power-up Initialization Sequence　… RESETの初期値は“L”がRecommend　⇒ **RZ/G1xでは非遵守**

3.3.2 Reset Initialization with Stable Power　… Mandatory　⇒ **RZ/G1xでは遵守**

3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.

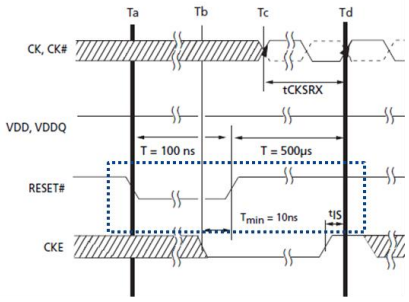


Reset and Initialization Sequence at Power-on Ramping

3.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2 * VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled "LOW" before RESET being de-asserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence steps 2 to 11.
3. The Reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



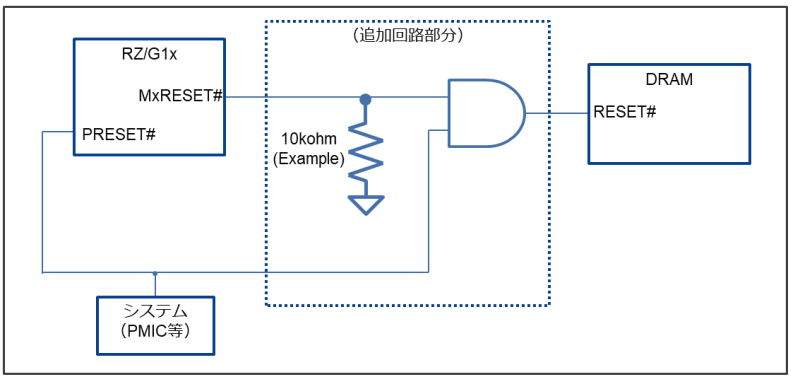
Reset Procedure at Power Stable Condition

想定される問題と対応策

電源投入時、RESET#が”H”だった場合、一部のDRAM製品では正常に初期化されない可能性があります。

特に、一部のDRAM製品では、電源安定後に再度RESET#による初期化を行っても、初期化が期待通りに動作しない場合があります。そのため、RZ/G1xではPull-down抵抗等でRESET#端子の初期状態を“L”にするなどの回路付加が必要になります。

以下に回路例を示します。



外部回路に関するご注意事項：

- 10kohmのプルダウン抵抗により、VDDQ_DDRの電流は最大0.158mA (=1.575V(DDR3_max)/10kohm) 増加します。