

# RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0133A/E	Rev.	1.00
Title	RZ/G2M V1.3 and G2M V3.0 Additional Explanations for Pin Multiplex		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2M V1.3, V3.0	Lot No.	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 Dedicated document for Pin Multiplex of RZ/G2M V1.3, V3.0 (EPMP-IMB-20-0058)		
		All lots				

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Additional explanations for "RZ/G Series, 2nd Generation User's Manual: Rev.1.11 Dedicated document for Pin Multiplex of RZ/G2M.

*Note: The pin function list reflected the changes of this technical update is attached to this document.*

[Priority level]

Importance: "Normal"

Urgency: "Normal"

[Products]

RZ/G2M V1.3, V3.0

[Section number and title]

Dedicated document for Pin Multiplexing [RZ/G2M V1.3, V3.0]

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. (Dedicated document) Pin Multiplexing [RZ/G2M V1.3, V3.0],

(\*1) after negate PRESET#, pin state is L output and then change to High output. regarding transition timing, please refer to the Reset section of H/W manual.

[pullup/pulldown control definition of pin]  
 pullup\* : pullup on/off is controllable in PFC register. Initial state is pullup on  
 \* : pullup on/off is controllable in PFC register. Initial state is pullup off  
 - : no pullup/pulldown  
 pulldown\* : pulldown on/off is controllable in PFC register. Initial state is pulldown on

(\*3) output value is H or L. this value depends on each chip.  
 (\*4) depends on MD21,MD20,MD11,MD10,MDT[1:0] setting  
 (\*5) depends on MD21,MD20,MD11,MD10,MDT[1:0] setting, in case JTAG interface is selected, "pullup" is selected. In case of other settings, ""(pullup on/off is controllable in PFC register. Initial state is pullup off) is selected.  
 (\*10) The initial value is [dnv2:drv1] = H3.  
 (\*11) The initial value is [dnv3:drv2:drv1] = H7.  
 (\*14) QSPI1\* = Z in case of MD[4:1]=0100 RZ/G2M Ver.1.3 only)  
 (\*15) In case of MD[4:1] = B'001x or B'101x (x: don't care), pin states of the QSPI1\_SPCLK and QSPI1\_SSL are as follows:  
 - During RPC\_RESET# is low level, QSPI1\_SPCLK is low output and QSPI1\_SSL is high output.  
 - During RPC\_RESET# is high level, QSPI1\_SPCLK is high output and QSPI1\_SSL is Hi-Z.

[symbol definition in "Handling when the Pin is not in Use"]  
 - : pin must be in use

(\*16) Do Not Use, these pins must be open (NDU: Do Not Use)  
 (\*17) The pin condition starts with the pin setting according to the boot device selected by the mode pin.  
 (\*18) In the case of an error at boot time, error log is output by using the SCIF pins.

Pin condition at PRESET#=L		Pin condition after power-on reset deassert				IO	drivability	pull-up/down controlled	schmitt	Power		Handling when the Pin is not in Use
initial pin setting	state	MD[4:1]=0000		MD[4:1]=others						Domain	Voltage	
USB3HS0_VBUS	Z	USB3HS0_VBUS	Z	USB3HS0_VBUS	Z					-	-	open
										VDD09_USB3HS0	0.8V	Power input
										VDDQ33_USB3HS0	3.3V	Power input
										VDDQ33_USB3HS1	3.3V	Power input
USB_EXTAL	I	USB_EXTAL	I	USB_EXTAL	I	I	-	-	-	VDDQ18	1.8V	open
USB_XTAL	O	USB_XTAL	O	USB_XTAL	O	O	-	-	-	VDDQ18	1.8V	open
ID0	Z	ID0	Z	ID0	Z					VDDQ33_USB2	3.3V	open
VBUS0	Z	VBUS0	Z	VBUS0	Z					-	-	open
DP0	Z	DP0	Z	DP0	Z					VDDQ33_USB2	3.3V	open
DM0	Z	DM0	Z	DM0	Z					VDDQ33_USB2	3.3V	open
TXRTUNE0	-	TXRTUNE0	-	TXRTUNE0	-					-	-	open
										VDD09_USB20	0.8V	Power input
										VDDQ33_USB2H0	3.3V	Power input
										VDDQ33_USB2	3.3V	Power input
ID1	Z	ID1	Z	ID1	Z					VDDQ33_USB2	3.3V	open
DP1	Z	DP1	Z	DP1	Z					VDDQ33_USB2	3.3V	open
DM1	Z	DM1	Z	DM1	Z					VDDQ33_USB2	3.3V	open
TXRTUNE1	-	TXRTUNE1	-	TXRTUNE1	-					-	-	open
										VDD09_USB21	0.8V	Power input
										VDDQ33_USB2H1	3.3V	Power input

Current (to):

(\*1) after negate PRESET#, pin state is L output and then change to High output. regarding transition timing, please refer to the Reset section of HW manual.

(\*3) output value is H or L, this value depends on each chip.

(\*4) depends on MD21.MD20.MD11.MD10.MD7[1:0] setting

(\*8) depends on MD21.MD20.MD11.MD10.MD7[1:0] setting, in case JTAG interface is selected, "pullup" is selected. In case of other settings, "" (pullup/on/off is controllable in PFC register. Initial state is pullup off) is selected.

(\*10) The initial value is [drv2drv1] = H3.

(\*11) The initial value is [drv3drv2drv1] = H7.

(\*14) QSPI1\* = Z in case of MD[4:1]=0100 RZ/G2M Ver.1.3 only)

(\*16) In case of MD[4:1] = B'001x or B'101x (x: don't care), pin states of the QSPI1\_SPCLK and QSPI1\_SSL are as follows:  
 - During RPC\_RESET# is low-level, QSPI1\_SPCLK is low output and QSPI1\_SSL is high output.  
 - During RPC\_RESET# is high-level, QSPI1\_SPCLK is high output and QSPI1\_SSL is Hi-Z.

[pullup/pulldown control definition of pin]  
 "pullup" : pullup/on/off is controllable in PFC register. Initial state is pullup on  
 - " : pullup/on/off is controllable in PFC register. Initial state is pullup off  
 - no pullup/pulldown  
 "pulldown" : pulldown/on/off is controllable in PFC register. Initial state is pulldown on

[symbol definition in "Handling when the Pin is not in Use"]  
 - : pin must be in use

(\*16) Do Not Use, these pins must be open (NDU: Do Not Use)  
 (\*17) The pin condition starts with the pin setting according to the boot device selected by the mode pin.  
 (\*18) In the case of an error at boot time, error log is output by using the SCIF pins.  
 (\*19) The USB data pins have their own pull-up/down control function.  
 Affected pins are as follows: USB3HS0\_DP and USB3HS0\_DM and DPn, DMn (n=0, 1). For more information, see Chapters 60.2, 60.7 to 60.8 and Chapters 61.2 to 61.3.  
 The processing of the USB USB-Data pins on the PCB must be designed in accordance with the PCB guidelines described in "Design Guidelines for Serial Interface Printed Circuit Boards with RZ/G2 Series Products".  
 Please contact Renesas Electronics Corporation for details about the Design Guidelines.

Pin condition at PRESET#~L		Pin condition after power-on reset deassert				IO	drive ability	pull-up/down controlled	schmitt	Power		Handling when the Pin is not in Use
		MD[4:1]=0000		MD[4:1]=others						Domain	Voltage	
initial pin setting	state	initial pin setting	state	initial pin setting	state							
USB3HS0_DP	Z	USB3HS0_DP	Z	USB3HS0_DP	Z			(*19)		VDDQ33_USB3HS0	3.3V	open
USB3HS0_DM	Z	USB3HS0_DM	Z	USB3HS0_DM	Z			(*19)		VDDQ33_USB3HS0	3.3V	open
USB3HS0_ID	Z	USB3HS0_ID	Z	USB3HS0_ID	Z					VDDQ33_USB3HS0	3.3V	open
USB3HS0_VBUS	Z	USB3HS0_VBUS	Z	USB3HS0_VBUS	Z					-	-	open
										VDD09_USB3HS0	0.8V	Power input
										VDDQ33_USB3HS0	3.3V	Power input
										VDDQ33_USB3HS0	3.3V	Power input
USB_EXTAL	I	USB_EXTAL	I	USB_EXTAL	I	I	-	-	-	VDDQ18	1.8V	open
USB_XTAL	O	USB_XTAL	O	USB_XTAL	O	O	-	-	-	VDDQ18	1.8V	open
ID0	Z	ID0	Z	ID0	Z					VDDQ33_USB2	3.3V	open
VBUS0	Z	VBUS0	Z	VBUS0	Z					-	-	open
DP0	Z	DP0	Z	DP0	Z			(*19)		VDDQ33_USB2	3.3V	open
DM0	Z	DM0	Z	DM0	Z			(*19)		VDDQ33_USB2	3.3V	open
TXRTUNE0	-	TXRTUNE0	-	TXRTUNE0	-					-	-	open
										VDD09_USB20	0.8V	Power input
										VDDQ33_USB2H0	3.3V	Power input
										VDDQ33_USB2	3.3V	Power input
ID1	Z	ID1	Z	ID1	Z					VDDQ33_USB2	3.3V	open
DP1	Z	DP1	Z	DP1	Z			(*19)		VDDQ33_USB2	3.3V	open
DM1	Z	DM1	Z	DM1	Z			(*19)		VDDQ33_USB2	3.3V	open
TXRTUNE1	-	TXRTUNE1	-	TXRTUNE1	-					-	-	open
										VDD09_USB21	0.8V	Power input
										VDDQ33_USB2H1	3.3V	Power input

[Description]

Note (\*19) for the USB data pins is added.

[Reason for Correction]

General error correction.

To avoid misunderstanding about IP pins internal pull-up/pull-down control.

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 End of Document -