[Notes]
RX Family QE for Display Module Firmware Integration Technology

R20TS1070EJ0100
Rev.1.00
Oct. 20, 2024

Outline

When using RX Family QE for Display Module Firmware Integration Technology (QE Display module), note the following points:

1. Notes on setting the buffer size (SCI_CFG_CHx_RX_BUFSIZ: x is channel) used for the receive queue of RX Family SCI Module Firmware Integration Technology
2. Notes on setting “Bit-endian of Output Data” and “Pixel Order of Output Data” on the “TCON/LCD Setting” tab of the QE for Display[RX] Standalone Version: Development Assistance Tool for Display Applications

1. Notes on setting the buffer size (SCI_CFG_CHx_RX_BUFSIZ: x is channel) used for the receive queue of RX Family SCI Module Firmware Integration Technology

1.1 Applicable Products

RX Family QE for Display Module Firmware Integration Technology Rev.1.00 (R01AN7283EJ0100)

1.2 Applicable Devices

RX651, RX65N Groups (ROM capacity: 1.5 MB to 2 MB)

RX66N Group

RX72N Group

RX72M Group

1.3 Details

The RX Family SCI Module Firmware Integration Technology (SCI Module) is used for communication with the QE for Display[RX] Standalone Version: Development Assistance Tool for Display Applications (QE for Display).

Setting the buffer size (SCI_CFG_CHx_RX_BUFSIZ: x is the channel) used for the receive queue of this SCI module to a specific value may cause problems in communication with QE for Display, making it impossible to perform LCD adjustments.

1.4 Conditions

Communication problems would occur if the buffer size (SCI_CFG_CHx_RX_BUFSIZ: x is the channel) used for the SCI module's receive queue is set to the following values:

124, 94, 83, 63, 42, 32

1.5 Workaround

Set the buffer size (SCI_CFG_CHx_RX_BUFSIZ: x is the channel) used for the receive queue of the SCI module to a value other than 124, 94, 83, 63, 42 or 32.

1.6 Schedule for Fixing the Problem

The problem has already been rectified in Rev.1.10. Please use Rev.1.10.

2. Notes on setting “Bit-endian of Output Data” and “Pixel Order of Output Data” on the “TCON/LCD Setting” tab of the QE for Display[RX] Standalone Version: Development Assistance Tool for Display Applications

2.1 Applicable Products

RX Family QE for Display Module Firmware Integration Technology Rev.1.00 (R01AN7283EJ0100)

2.2 Applicable Devices

RX651, RX65N Groups (ROM capacity: 1.5 MB to 2 MB)

RX66N Group

RX72N Group

RX72M Group

2.3 Details

“Bit-endian of Output Data” and “Pixel Order of Output Data”are not set correctly on the “TCON/LCD Setting” tab of the QE for Display.

2.4 Conditions

The problem would always occur.

2.5 Workaround

Refer to the following function in r_qe_display_lcdc.c, and change according to the red text.

Before modification

```
static void r_set_display_param_output(uint8_t * p_data)
{
    uint32_t temp;


(Omitted)
    /* Back ground color */
    temp = (uint32_t) (((*(p_data + 2)) << 16) | ((*(p_data + 1)) << 8) |
(*p_data));
    s_display_cfg.output.bg_color.argb = temp;
    p_data += 3;
(Omitted)
}
```

After modification

```
static void r_set_display_param_output(uint8_t * p_data)
{
    uint32_t temp;


(Omitted)
    /* Back ground color */
    temp = (uint32_t) (((*(p_data + 2)) << 16) | ((*(p_data + 1)) << 8) |
(*p_data));
    s_display_cfg.output.bg_color.argb = temp;
    p_data += 4;
(Omitted)
}
```

2.6 Schedule for Fixing the Problem

The problem has already been rectified in Rev.1.10. Please use Rev.1.10.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct.20.24	-	First edition issued

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