The Fundamental Advantages of Normally-Off D-Mode GaN

A Brief Tutorial Outlining the Superior Benefits of D-Mode versus E-Mode GaN

Inarguably, GaN power semiconductors are a hot topic in power electronics. Two transistor variations prevail today: normally-off d-mode GaN and e-mode GaN.

When confronted with the choice, the debate at times inexplicably leans toward e-mode. In reality, normally-off d-mode GaN proves to be a fundamentally superior platform in performance, reliability, versatility, manufacturability, and practical application. The reasoning lies in the normally-off d-mode's ability to capitalize on the inherent advantages of the GaN material.

Nature's Gift from GaN: The 2DEG

GaN transistors are successful largely because of one key natural phenomenon: the 2-dimensional electron gas (2DEG) channel. The 2DEG is an incredibly fast channel that spontaneously forms at the interface between the GaN and a thin AlGaN layer. Its electron density is amongst the highest naturally occurring in semiconductors. It also offers high mobility at 2000 $cm^2/V{\cdot}s$, which is twice that of state-of-the-art silicon (Si) and silicon carbide (SiC) devices. As a result, the 2DEG yields an impressively low resistance-versus-capacitance figure of merit with record-high efficiency.

Every GaN Power Semiconductor Starts as a D-Mode Device

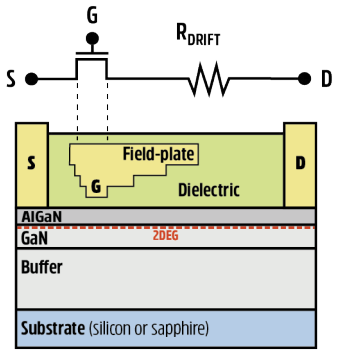


Figure 1: *The ultimate embodiment of a GaN power transistor—a depletion-mode AlGaN/GaN High-Electron Mobility Transistor (HEMT).*

Figure 1 shows the archetypal form of a lateral GaN power transistor; lateral being the structure of virtually every GaN device on the market today. The AlGaN/GaN layers are deposited on a silicon substrate and separated by an engineered buffer to achieve high material quality and blocking voltage. The channel is contacted by the source and drain terminals to enable current to flow between the source and drain contacts. The gate terminal modulating the current is located between the source and drain terminals and is isolated with a dielectric stack to ensure low leakage and high robustness. A field-plate structure is designed for best electric field spreading and highest reliability.

Thanks to the material's nature, the 2DEG channel at the AlGaN/GaN interface forms *spontaneously*, with no need for external gate bias. This means **the device is normally on** and requires a negative gate bias to deplete the channel and turn off. It is, in fact, a depletion mode (d-mode) device. But power electronic systems require normally-off devices for fail-safe operations.

The question then becomes how to make the lateral GaN HEMT normally off? This is where normally-off d-mode and e-mode (p-GaN gate) technologies part ways.

In the normally-off d-mode technology, the GaN HEMT is untouched to retain its highest performance and reliability. In its natural state, the 2DEG channel is free to maximize its unparalleled combination of high mobility and charge density. Renesas' normally-off d-mode approach pairs the GaN HEMT with a low-voltage, normally-off Si MOSFET to achieve normally-off operation. This solution provides a positive threshold voltage of 2.5 V to 4.0 V depending on power level, topology, and system architecture.

Alternatively, an e-mode approach opts to control the 2DEG channel inside the HEMT itself—a design decision that negatively impacts the 2DEG's advantage.

E-Mode GaN Throttles the 2DEG's Natural Benefits

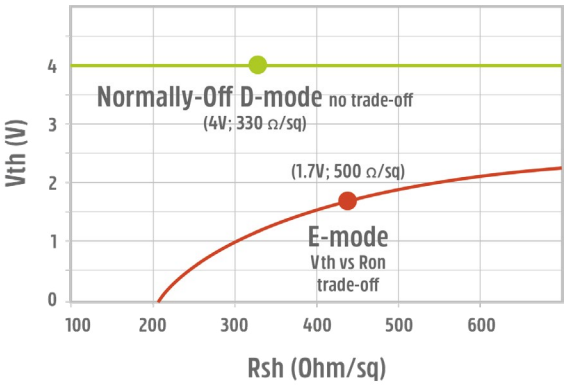


Figure 2: *Higher sheet resistance results from starting with lower channel charge needed to pinch off the channel.*

When power engineers modify a lateral GaN HEMT to achieve normally-off behavior, critical compromises are made. First, the 2DEG's charge density must be reduced, which generates a higher resistance per unit area [Figure 2] and lower figure of merit than achieved in its natural state.

Second, a p-type doped GaN layer [Figure 3] must be added under the gate metal. The p-GaN layer serves as a built-in negative battery (approximately -3.2 V) that turns the 2DEG channel off and yields a barely positive threshold voltage of approximately 1.6 V.

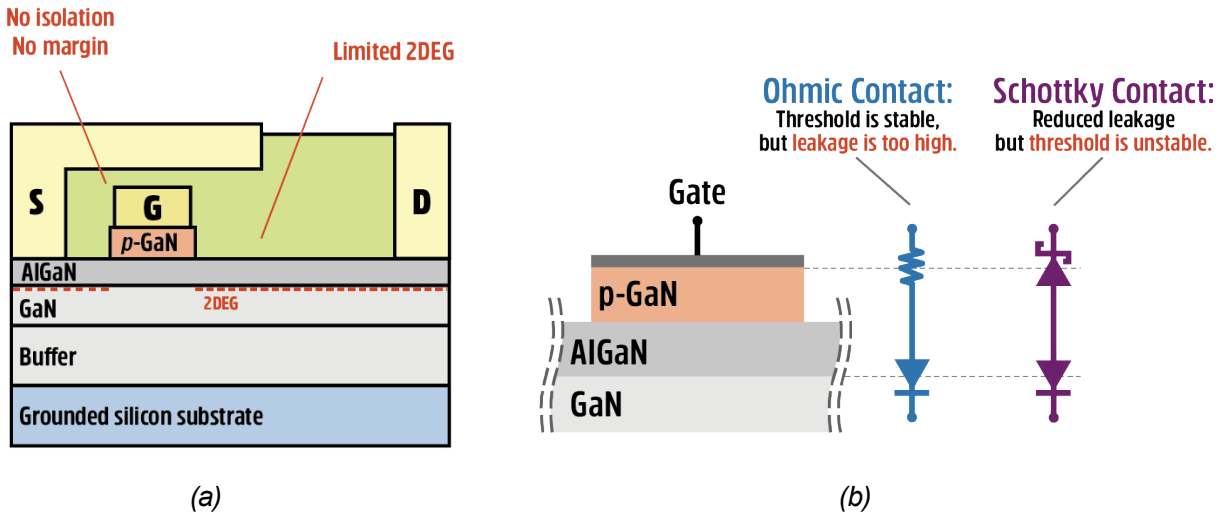


Figure 3: *(a) e-mode (p-GaN gate) structure, showing no gate isolation. (b) Schematic showing Schottky metal contact, yielding a dangerous back-to-back diode with floating p-GaN layer in between leading to dynamic Vth issues.*

When dealing with noisy environments or high-power levels, a 1.6 V threshold may not be enough. A negative gate drive of approximately -3 V will then likely be used, adding circuit complexity and additional dead-time loss. In fact, with a gate bias of -3 V, the reverse current flowing from source to drain must overcome the negative gate voltage which causes additional undesired power loss. Notably, the negative drive's negative impact on the dynamic or switching resistance of the device (which is the relevant resistance in the application) is not taken into account in e-mode device datasheets and is a major topic of study and concern.[1]

The Domino Effect: E-Mode's Lack of Isolation, Dynamic Threshold Issues, Low Performance, and Fragility

The e-mode modifications indicated above come at a cost: the loss of gate isolation…and more.

Replacing the gate dielectric with p-type GaN results in the gate no longer being isolated. Which, in turn, causes a significant gate current under positive bias, posing severe constraints to maximum gate voltage ratings. To reduce that significant gate current, yet another modification is made: the gate contact is changed from an ohmic metal to a Schottky barrier [Figure 3B].

The Schottky barrier then introduces still another challenge as it now hinders the discharge of the gate-drain capacitance during turn-on transient. This, in turn, leads to a detrimental phenomenon referred to as "dynamic threshold" (reported by several research groups[2, 3]) which causes dynamic on-state resistance issues as shown in Figure 4. At a voltage of 480 V, an e-mode device shows a dynamic RDS(on) increase of 27%, whereas its normally-off d-mode counterpart shows only 5% resulting in less conduction losses. The e-mode data reported in Figure 4 is consistent with what's shown in independent research studies.[4]

1 J. Wei et al., "Dynamic Threshold Voltage in p-GaN Gate HEMT," 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 2019, pp. 291-294, doi: 10.1109/ISPSD.2019.8757602..
2 Ibid.
3 A. Chini et al., "Gate-Bias Induced RON Instability in p-GaN Power HEMTs," in IEEE Electron Device Letters, vol. 44, no. 6, pp. 915-918, June 2023, doi: 10.1109/LED.2023.3265503.
4 Zhong et al., "IG- and VGS-Dependent Dynamic RON Characterization of Commercial High-Voltage p-GaN Gate Power HEMTs" Digital Object Identifier 10.1109/TIE.2021.3104592.

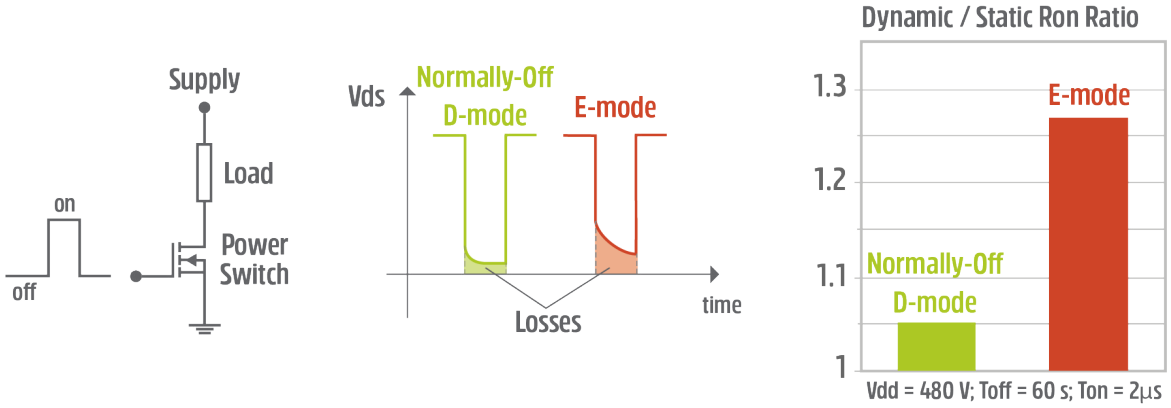


Figure 4: *e-mode devices with Schottky barriers have difficulties discharging device capacitance, causing dynamic threshold and on-state resistance issues as well as higher losses.*

Due to difficulty in discharging the capacitance, the e-mode device's threshold voltage is now unstable during switching. This results in higher power losses versus its normally-off d-mode counterpart. (Note: This is likely why e-mode manufacturers do not typically report dynamic RDS(on) ratings.) To mitigate this problem, one could theoretically overdrive the gate to reduce the RDS(on) of the device under the gate. However, this potential solution is up against a very tight voltage window as it must comply with a small gate maximum rating to prevent gate damage (max 7 V) [Figure 5].

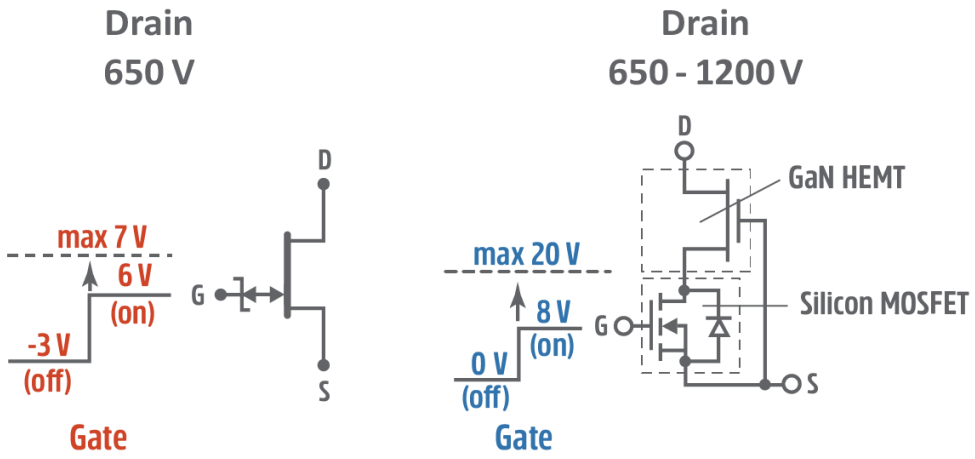
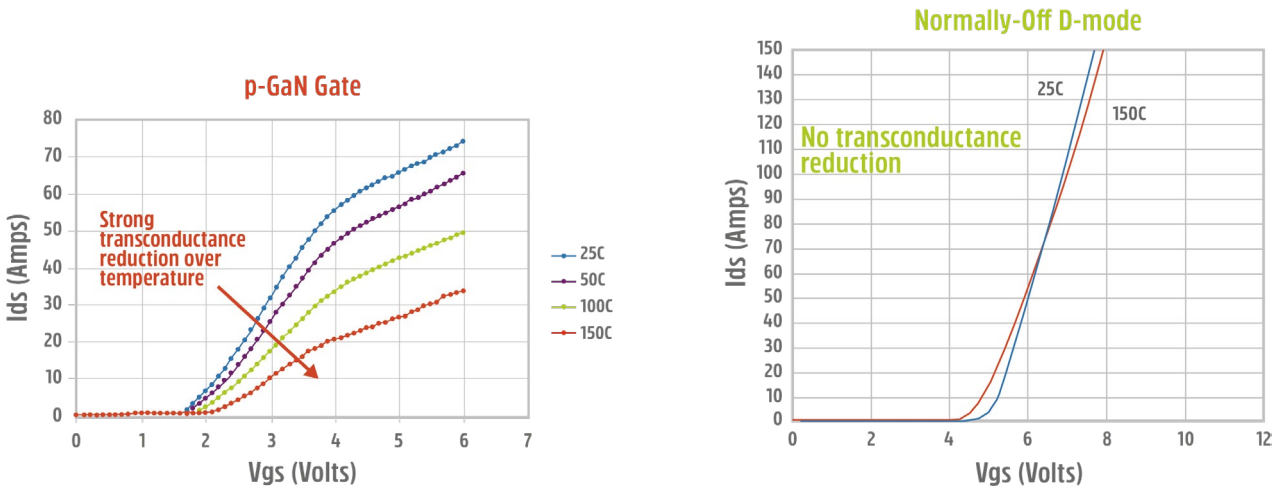


Figure 5: *e-mode drive to fully enhance the channel is sensitive to damage due to only 1 V of headroom.*

Additionally, as temperature rises during normal device operations, the 2DEG mobility naturally decreases.

The reduction in 2DEG mobility over temperature also causes the p-GaN gate transconductance to drop [Figure 6], resulting in even slower transitions and still more switching losses[5] versus that of normally-off d-mode GaN. The decrease creates the perfect storm for low efficiency. To manage these issues, a p-GaN gate solution would need to start with a larger die which still presents the problem of increased Miller capacitances reducing overall efficiency and higher cost.

5 S. I. H. Sabzevari, S. Abdi and R. Ghazi, "Assessment of the Switching Characteristics of a commercial e-mode Power GaN Device Using a Dual Pulse Test Set-up," 2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Florence, Italy, 2021, pp. 1-6, doi: 10.1109/CPE-POWERENG50821.2021.9501072.



(a) *(b)*

Figure 6: *(a) p-GaN Gate transconductance increases over temperature and reduces gate drive capability. (b) normally-off d-mode GaN has no degradation in transconductance over temperature because the silicon gate is independent from GaN mobility droop at high temp.*

Per datasheet ratings, the e-mode device's on-state resistance shows a higher temperature coefficient than normally-off d-mode. In fact, it's as high as 2.6x between 25°C and 150°C [Figure 7], yielding a rapid increase of conduction losses.

The e-mode design constraints continue with the susceptibility of threshold voltage drift due to trap injection into the buffer. e-mode's silicon substrate must connect to the source terminal to mitigate buffer charging caused by electron injections from the source itself.

This modification restricts e-mode's drain voltage maximum rating to 650 V. Given that higher voltages require thicker GaN buffers to support the substrate-to-source connection, e-mode devices are essentially left behind in the race to 1200 V as thicker GaN buffers require more sophisticated technology…which adds still more cost.

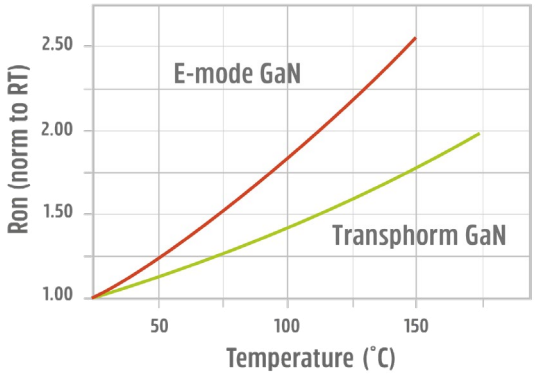


Figure 7: *Renesas' normally-off d-mode GaN shows superior temperature coefficient of resistance versus p-GaN gate HEMTs.*

The Normally-off d-mode Philosophy: The Right Approach for the Right Purpose

Transphorm, now Renesas Electronics Corporation, approaches GaN power semiconductors differently. Again, its platform pairs the normally-on GaN HEMT with a highly reliable, highly performant normally-off low-voltage Si MOSFET in a normally-off d-mode configuration. This ensures the platform's fail-safe normally-off operations while retaining highest GaN performance and highest Si MOSFET gate reliability.

Developing a normally-off d-mode GaN platform was deliberate for various reasons; the most important two being that it works synergistically with nature and is backward compatible with today's silicon technology. As stated earlier, it allows platform elements—particularly the 2DEG—to do what they do best. So, instead of limiting GaN's

advantages via e-mode (p-GaN gates), normally-off d-mode embraces GaN's potential. And the resulting normally-off d-mode platform stands as a high performing, highly robust GaN technology with industry-leading reliability and versatility.

Leveraging D-Mode's Natural Advantages

Normally-off d-mode devices do not face the aforementioned challenges experienced by e-mode devices. For example, the normally-off d-mode solution is unaffected by dynamic threshold issues since one drives a gate-isolated low-voltage Si MOSFET. The threshold voltage is set by the Si MOSFET independent of the GaN HEMT.

The normally off normally-off d-mode d-mode configuration also generates a second gift from nature in addition to the 2DEG: the SiO2/Si interface. This interface naturally isolates the device gate, offering the automotive-grade maximum gate rating of +/- 20 V with exceptional reliability and high drive margin. The threshold voltage is as high as 4 V, with no compromises on the 2DEG. The low-voltage Si MOSFET does not require negative bias or any special gate drivers. It is stable under all switching conditions, with no hidden power loss associated with dynamic threshold issues. As can be seen in Figure 6B, the transconductance of normally-off d-mode GaN devices is exceptionally high and doesn't drop with temperature because it is set by the Si MOSFET and independent from the 2DEG mobility.

These advantages are backed by real-world data. When Renesas' SuperGaN® normally-off d-mode devices replaced the original e-mode GaN devices shipped in a commercially available power adapter, the SuperGaN FETs delivered higher efficiency and up to 50% lower case temperature despite having a smaller chip size and a 30% higher on-resistance rating [Figure 8].

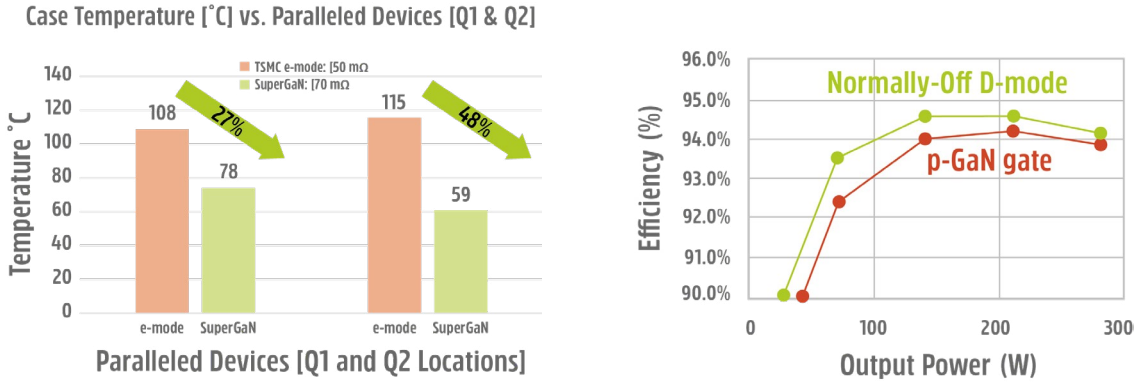


Figure 8: *280 W Razer power supply performance difference between SuperGaN and p-GaN gate HEMTs.*

MYTH #1

Si MOSFETs add on-state resistance and reverse recovery charge.

Reality: In normally-off d-mode GaN technology, the GaN chip bears most of the off-state high voltage (> 90%). The Si MOSFET needs only to bear a few 10's of volts. And, as the specific on-state resistance per unit area decreases quadratically with rated voltage, the Si MOSFET achieves incredibly low RDS(on), less than 10% of the total normally-off d-mode resistance, and very small reverse recovery charge (Qrr). Notably, that Qrr is an order of magnitude lower than high voltage superjunction Si MOSFET technology. To put things in perspective, if we take a conventional 600 V Si superjunction power device, the resistance-versus-charge figure of merit (Ron * Qrr) is 145 mΩ-pC. If we take a 650 V normally-off d-mode GaN, the figure of merit drops to 6 mΩ-pC, marking a huge improvement. And of 6 mΩ-pC, the low voltage Si MOSFET contributes only 0.5 mΩ-pC—less than 10% of the total normally-off d-mode GaN, and less than 0.5% of the 600 V silicon power device [Figure A]. ***Myth busted!***

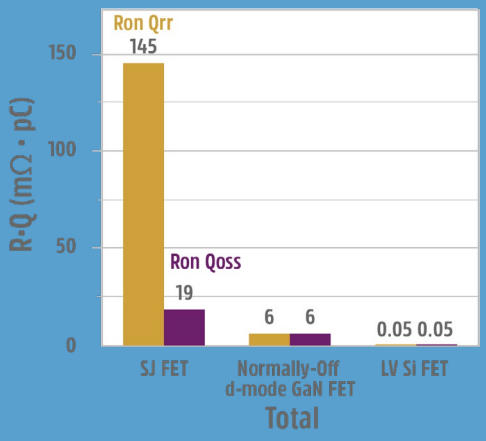


Figure A: *Switching figures of merit of 600 V Si superjunction devices, 650 V normally-off d-mode GaN devices, and low-voltage Si FETs paired with the GaN HEMT. The low-voltage Si FET adds minimal contribution to the overall normally-off d-mode GaN resistance and capacitance.*

High Temperature Reverse Bias with Dynamic On-Resistance Testing

As with all semiconductors, discrete power devices undergo several qualification tests to ensure that their quality, reliability, and performance meet basic industry requirements. One of the most common JEDEC and AEC-Q101 qualification tests is the High Temperature Reverse Bias (HTRB)—a standard intrinsic (lifetime) reliability assessment.

MYTH #2

e-mode devices have no Qrr.

Reality: When switching from reverse conduction to off-state, the reverse recovery charge accounts for not only bipolar transport minority carriers recombination, but also the formation of the space-charge region which is effectively equivalent to the output charge (Qoss). It's true that GaN HEMTs have no reverse conduction bipolar transport, but they nevertheless do have output capacitance that needs to be charged during reverse recovery. In a nutshell, Qrr = Qoss. Qrr cannot be zero. ***Myth busted!***

Specifically, the HTRB test evaluates the long-term reliability by accelerating any failure mechanisms that might be present in the devices. The devices are placed under high drain-source bias (i.e., 80 or 100 percent of the rated voltage) while at a high junction temperature of 150°C or 175°C. Typical HTRB test read points are 250 hours, 500 hours, and 1,000 hours (6 weeks) [Figure 9].

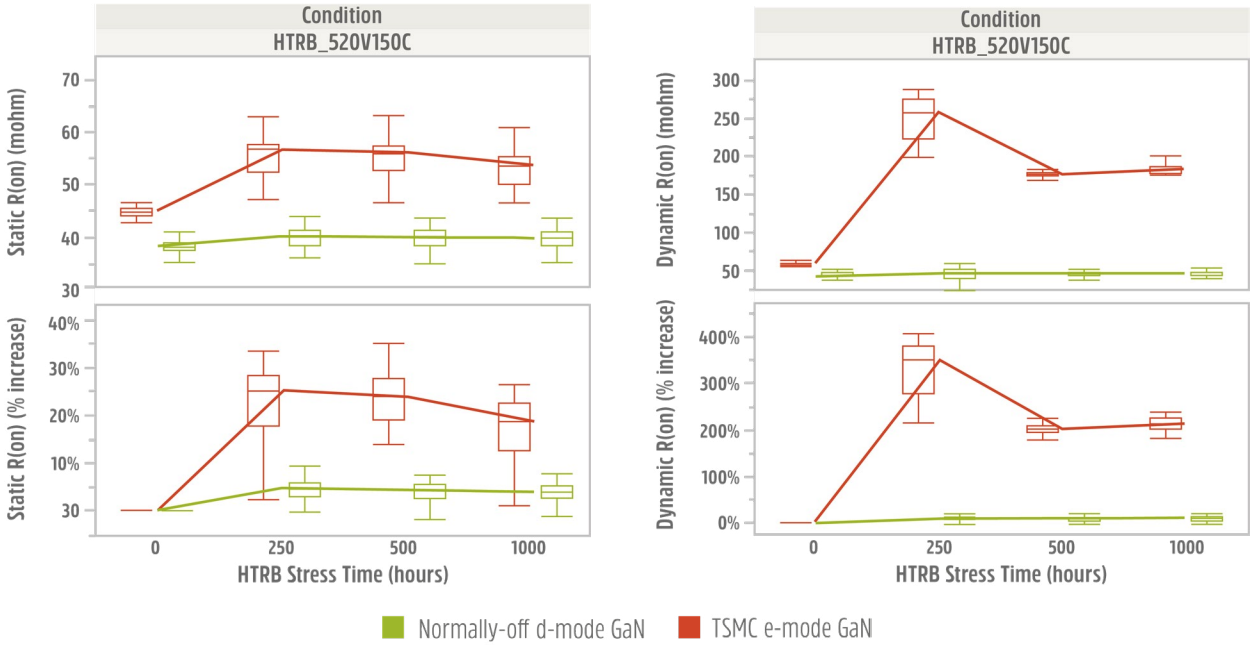


Figure 9: *Normally-off d-mode GaN vs. TSMC e-mode GaN static on-resistance (Figure 9a) and dynamic on-resistance (Figure 9b).*

MYTH #3

Normally-off d-mode GaN oscillates.

Reality: Normally-off d-mode GaN has a lot of gain. And gain is a wonderful thing, leading to very fast switching. But it needs to be harnessed properly to achieve the desired performance while preventing undesired effects, such as oscillations. To prevent oscillations and to get the most out of any fast-switching semiconductor device, circuit engineers should follow standard design principles, such as: minimizing gate and power loop inductances, selecting the correct gate resistor(s) and gate ferrite bead, and/or deploying RC snubbers where needed (mostly at the DC link, as close as possible to the drain terminal of the device). All of these design principles are simple to implement and are summarized in Application Note AN0009.[1] If properly implemented, they do not degrade the GaN HEMT's performance. On the contrary, they enhance it while suppressing oscillations and electromagnetic interferences (EMI). See waveforms in Figure B. ***Myth Busted!***

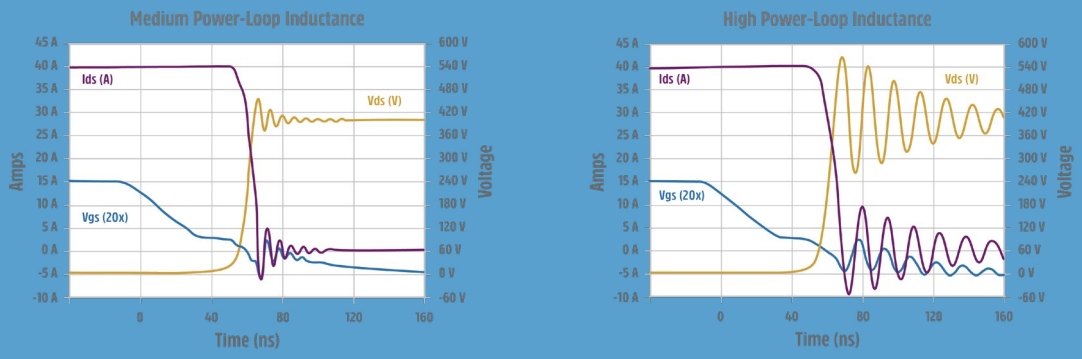


Figure B: *Normally-off d-mode GaN devices have high gain. Good circuit design with optimized power loop inductance helps suppress oscillations and achieve fast switching and high performance.*

1 See App Note Recommended External Circuitry for Renesas GaN FETs.

HTRB testing was conducted on Renesas' 50 mΩ normally-off d-mode SuperGaN device and a comparable TSMC e-mode device. The HTRB conditions used were 520 V @ 150°C for 1000 hours followed by both a static and dynamic [Figure 10] on-resistance test to verify each FET's datasheet specifications.

The two on-resistance tests (static and dynamic) were done after each time interval [Figure 10]. As indicated in Figure 9a, the e-mode device demonstrates a rise (~30%) in on resistance during static testing. This could be charge trapped in the dielectric layer (i.e., passivation layer) with such a long recovery time that it registers in the static test.

When analyzing the dynamic on-resistance results, Figure 9b shows the e-mode device experiencing a more than 300% rise in on resistance. It is unclear exactly why this occurs during the e-mode FET's dynamic switching tests. However, it is likely a design, process, or epi issue.

What is known is that both normally-off d-mode and e-mode GaN FETs experience current collapse also known as

electron charge trapping in the GaN HEMT structure itself, which is comprised of the buffer, GaN, AlGaN, 2DEG channel, and other layers [Figure 1]. Charge trapping affects dynamic on resistance and may also impact static on resistance.

Relying on static on-resistance ratings alone may not always provide an accurate read on the key GaN design specification responsible for conduction losses (RDS(on)). Testing dynamically is a way to measure charge trapping and overall on-resistance stability.

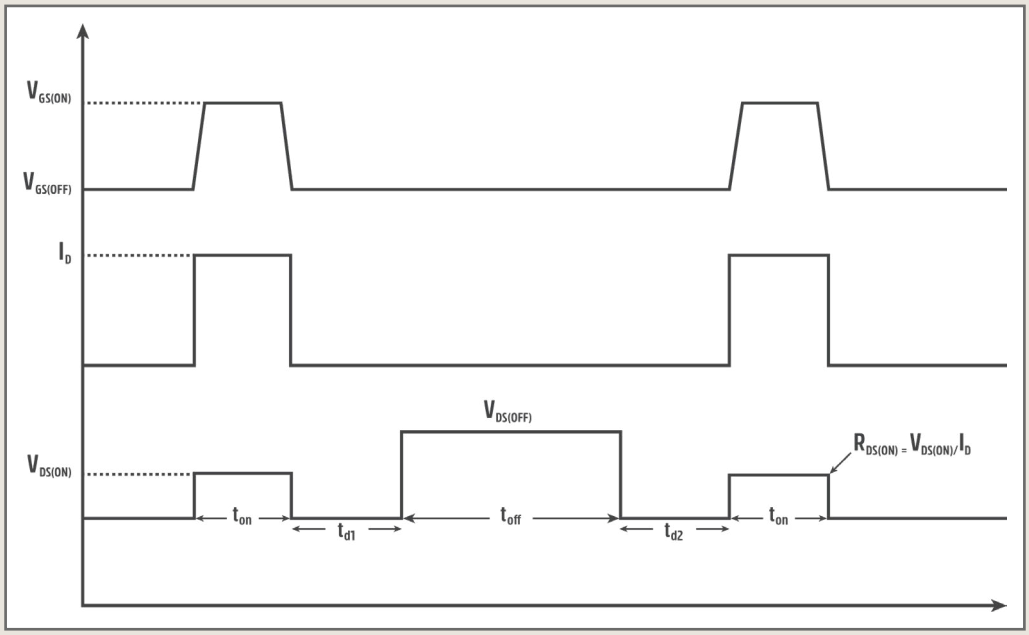


Figure 10: *Example of a timing diagram for measuring dynamic on-resistance.*
(Source: JEDEC, JEP173; "Dynamic On-Resistance Test Method Guidelines for GaN HEMT Based Power Conversion Devices.")

Table 1 below provides a numerical representation of Figure 9's static and dynamic plot points against each device's published datasheet specifications.

Supplier	Datasheet Typical RDS(on) (25°C)	Datasheet Maximum RDS(on) (25°C)	Tested Static RDS(on) 0/250/500/1000 hrs	Tested Dynamic RDS(on) 0/250/500/1000 hrs
Renesas *normally-off d-mode*	50 mΩ	60 mΩ	38.2/39.4/39.2/39.4	39.9/43.3/43.3/43.6
TSMC *e-mode*	50 mΩ	68 mΩ	44.6/59.6/53.2/50.1	57.4/151.9/158.9/157

Table 1: *Static and dynamic on-resistance at 0, 250, 500, and 1,000 hours of HTRB*

The results charted in the table underscore a critical fact: datasheets do not always state a device's true figure-of-merit (FOM) as seen on the bench. Meaning, generally, design engineers must carefully consider relying on datasheets published with static on-resistance values given there may be high variability—an issue that could ultimately result in reliability issues with in-production power systems.

An additional takeaway: the HTRB test results show that the TSMC e-mode device's dynamic on-resistance would fail AEC-Q101 qualification based on e-mode exhibiting a more than 20 percent shift pre-to-post based on its typical datasheet value. That value discrepancy will likely impact the specified maximum rated current, causing additional device power loss which, in turn, results in temperature rise and reliability issues over time.

Renesas, being a vertically integrated company that owns its design, epi manufacturing, and wafer processing, has minimized the above e-mode issues with its normally-off d-mode devices. These reliability advantages are directly attributed to the Renesas GaN platform's fundamental physics defined at the start of this paper. In fact, the normally-off d-mode device rates better than indicated by its datasheet's conservative specifications—thereby showing greater device stability that maximizes the lifetime reliability of end products.

GaN Package Versatility Equals Customer Application Compatibility

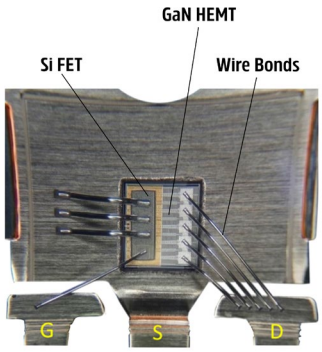


Figure 11: *SuperGaN FET die-on-die assembly (TO-247 test vehicle). Can be done in surface mount packages, like PQFN, TOLL, TOLT, or modules.*

The normally-off d-mode platform fits elegantly in a broad range of standard packages such as through-holes, surface mounts, and multi-chip modules. These packages are considered high performing and highly reliable in their own right, adding to the performance and reliability of the GaN platform itself.

With modern assembly and packaging technologies, the parasitic inductances of Renesas' high power normally-off d-mode products are minimized. In fact, Renesas' SuperGaN normally-off d-mode platform features a die-on-die technology with silicon-like wire bonding [Figure 11]. No additional wire-bonds or parasitic inductance are added which allows for the desired connection scheme including wire bond, copper clip, and Kelvin source.

The normally-off d-mode configuration also lends itself beautifully to system-in-package integration, where the gate driver and controller are integrated seamlessly with the d-mode HEMT and low-voltage Si MOSFET (monolithically or hybrid)—adding still another option to satisfy diverse end application requirements.

Additional Considerations

The normally-off d-mode GaN HEMT does not need to connect the source to the substrate. A floating or insulating substrate enables a higher voltage rating (ex: up to 1200 V[6]) and bidirectional switch implementation.[7]

Interestingly, if one wants to develop a bidirectional switch using p-GaN gates, they will face yet another difficult decision: As both terminals alternate their polarity from ground to DC bus voltage, which terminal should the substrate connect to? It's a question with no clear answer.

Normally-off d-mode GaN HEMTs deliver one more critical advantage not readily accessible to e-mode HEMTs today.

As GaN transistors penetrate the motor drive market, short-circuit capability will be required. D-mode's insulated gate voltage handling allows for very elegant design methods. Such methods are proven to tailor the short-circuit withstand time (SCWT) of Renesas' d-mode devices up to 5 microseconds,[8] meeting the requirements of commercially available gate drivers. Renesas achieves SCWT through its proprietary semiconductor process without adding additional masks or current sensing pins—making three-leaded packages still applicable. To date, e-mode does not seem fully prepared for this eventuality with demonstrations being limited and sometimes misleading.

Conclusion

When considering the above listed advantages and others, the normally-off d-mode platform generates a portfolio of GaN devices that optimize and magnify the inherent advantages of GaN as a semiconductor material—producing a truly revolutionary power conversion solution for next generation power electronics.

Visit renesas.com/GaN for more information including design resources, full datasheets and samples.

6 G. Gupta et al., "1200V GaN Switches on Sapphire Substrate," 2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vancouver, BC, Canada, 2022, pp. 349-352, doi: 10.1109/ISPSD49238.2022.9813640.
7 J. Huber and J. W. Kolar, "Monolithic Bidirectional Power Transistors," in IEEE Power Electronics Magazine, vol. 10, no. 1, pp. 28-38, March 2023, doi: 10.1109/MPEL.2023.3234747.
8 D. Bisi et al., "Short-Circuit Capability with GaN HEMTs : Invited," 2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2022, pp. 1-7, doi: 10.1109/IRPS48227.2022.9764492.

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan
https://www.renesas.com

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