It’s All about the Money!

Reducing Costs of IO-Link Master Designs with the CCE4511

Abstract

In industrial automation, IO-Link is an extremely fast-growing standard to connect sensors and actuators to the higher-level control/monitoring system. IO-Link Masters are typically used as gateways and can interface multiple IO-Link devices and non-IO-Link devices by a point-to-point connection. One of the key benefits of IO-Link is the competitive pricing. To help designers develop a cost-efficient IO-Link Master, this white paper explains why using the CCE4511 4-Channel Master Transceiver reduces development costs and bill-of-materials (BOM) costs.

Introduction of the CCE4511

The CCE4511 is a state of the art 4-Channel IO-Link Master Transceiver, offering a broad spectrum of features and benefits. It perfectly complements Renesas' existing product portfolio, which already includes IO-Link Master and Device Transceivers for various application scenarios.

With 4 full IO-Link compliant channels with a continuous CQ driving current of up to 500 mA, an integrated Frame Handler, Ready Pulse Detection, 8 LED drivers and various protection features, the CCE4511 offers everything needed to design a robust, reliable and cost-efficient multi-channel-IO-Link Master unit.

The SPI interface allows configuring the registers and controlling the channels, while the integrated UART interfaces enable direct control for each IO-Link channel.

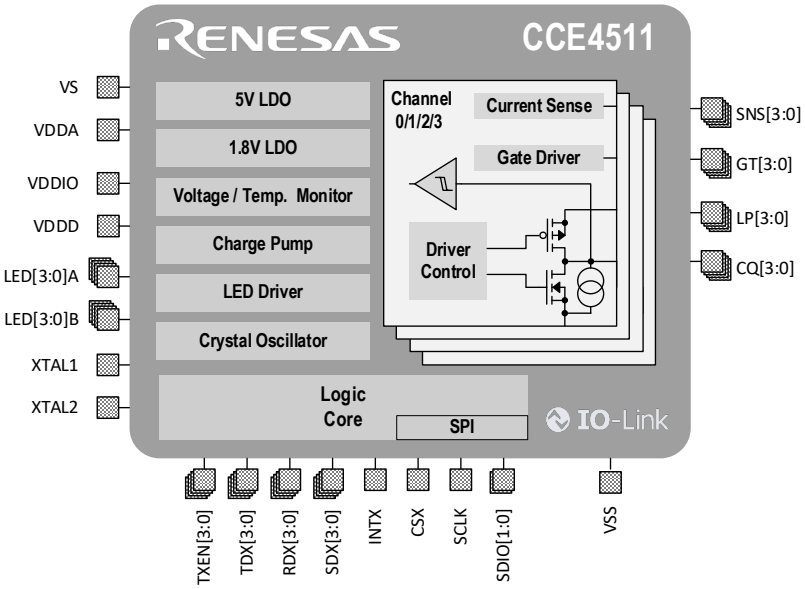

Figure 1: CCE4511 block diagram

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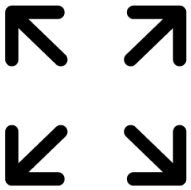
Its wide supply voltage range of 8 to 36 VDC for the high voltage supply, and 1.8 to 5 VDC for the digital supply, combined with the wide operating temperature range of -40 to +125°C, facilitates its use in an extensive range of applications.

The CCE4511 is available in a QFN56 package, measuring only 8 mm x 8 mm, thus contributing significantly to a PCB space-saving IO-Link Master design.

Aspects of Cost Saving

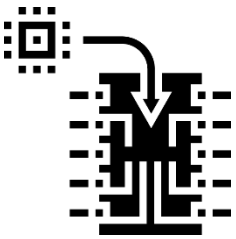
When designing a PCB, no matter the purpose of the PCB, different aspects need to be considered when cost and size of the final product are a key factor. These aspects are, for example, PCB dimensions, the bill of materials, design efforts, and manufacturing costs, but also aspects like the available features of the chosen components.

With the CCE4511 and its built-in features, the cost driving aspects of an IO-Link Master Design can be reduced.



PCB Dimensions

With four full IO-Link compliant channels and the small QFN56 (8 mm x 8mm) package, the CCE4511 actively contributes to reduce the size of the PCB. Other IO-Link Master Transceivers typically have only 2 channels and a package size of about 7 mm x 7 mm, which results in a total area of 98 mm² if four IO-Link channels are designed (for the master transceivers only). The CCE4511 results in a total area needed of only 64 mm², thus saving already about 35% of PCB space. Additionally, external circuitry can be reduced, saving even more valuable PCB space and BOM costs while further reducing design efforts in the PCB layout.



Built-in Features

Built-in features can have a significant impact on the design and design decisions. The CCE4511 offers a variety of different features, that can help reducing the costs of the design.

The integrated Frame Handler, which was developed in cooperation with TMG TE to optimize it, aims to reduce the load for the microcontroller by automated calculation of checksums, check IO-Link timing constraints, and store input or output data which helps to comply with IO-Link cycle times. By reducing the load of the microcontroller, it is possible to select from a broader range of less performant microcontrollers and thus reducing BOM cost.

The CCE4511 offers two integrated LED drivers per channel, which can be configured via register settings. This eliminates the need for current-limiting resistors and available pins at the microcontroller (or any other external LED driver IC).

Another feature that supports the reduction of software development efforts and enables the CCE4511 to be used within IO-Link Safety applications, is the integrated Ready Pulse Detection. With this feature, the CCE4511 can automatically detect the ready pulse, which is sent by the IO-Link Safety Device to confirm it has passed all internal safety checks and is ready to detect the IO-Link wake-up sequence from the IO-Link Master. An automated IO-Link wake-up sequence generation is also integrated in the CCE4511.

Depending on the application, other features (e.g. protection features) of the CCE4511 might contribute to reduced design efforts or BOM cost reductions, and therefore reducing the overall design costs.

Bill of Materials

Reducing the number of components used in a design will not only reduce cost of the design, but will also lead to a more secure procurement process. Of course, BOM comparison is a fairly difficult task, since the features and specifications of available IO-Link master transceivers differ, but when comparing with competitors at a minimum functionality level, the CCE4511 does need fewer external components to support 4 fully IO-Link compliant channels. In addition to the quantity of components, the price of each component is a decisive factor. Compared to other IO-Link master transceivers, the CCE4511 offers a significant lower price per IO-Link channel.

Design Efforts

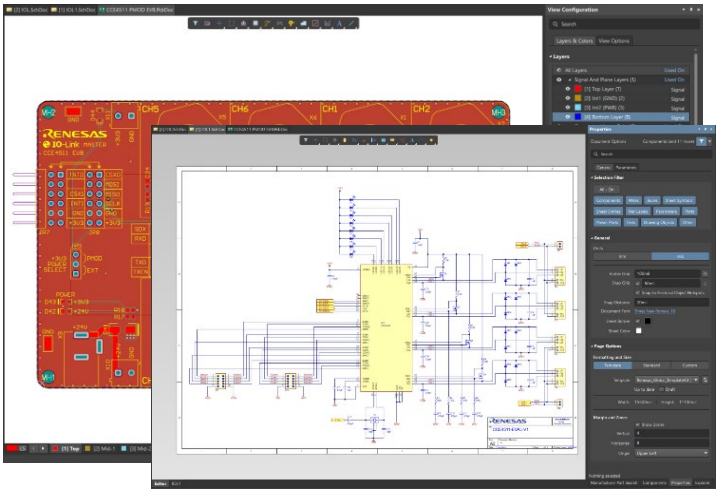
Design efforts are a major contributor to the costs of PCB design. We understand the time needed to do schematic design and PCB layout, software development, test of the design, and writing necessary documentation. With the CCE4511, less components (including the IO-Link master transceiver) are needed, which results in a reduced effort for schematic design and PCB layout. Some of the CCE4511's features, such as the integrated Frame Handler, also help reduce development effort, especially in software development. Additional resources like a hardware application note and an evaluation board are available to speed up the design.

Speed up the Design

To help customers to speed up the design process of IO-Link Masters with the CCE4511, Renesas offers technical support and guidance, as well as evaluation boards and application notes.

Figure 2: CCE4511-EVAL-V1

The CCE4511-EVAL-V1 can be used with any suitable external MCU, preferably with a Pmod interface, like the YCONNECT-IT-RZN2L. It has 8 IO-Link channels, which is a common channel count for industry standard IO-Link Masters, additional protection circuitry and a flexible power supply.



Renesas also offers the Altium Board and schematic files, enabling customers to inspect and implement them in their own designs.

Besides the evaluation board and Altium files, the available application note can help the customer make hardware design decisions. All documentation and files are available on the Renesas website for download.

Summary

In a modern industrial environment, where the focus of product development is increasingly on cost and time-to-market, it is important to carefully evaluate all design decisions. In this White Paper, Renesas provided information on how to reduce costs of an IO-Link Master design using the new CCE4511 4-Channel Master Transceiver. The CCE4511 offers great potential in terms of cost reduction and features, and is the industries' first master transceiver integrating IO-Link safety features.

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