White Paper

Space Grade Power Solution for the Microchip® RTG4™ FPGA

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Abstract

Over the last decade satellites and spacecrafts have seen an exponential increase in the need for on-board data processing and storage demands. Additionally, major satellite manufacturers have recently announced their latest satellites to be modular, fully digital and capable of in-orbit reconfigurability. To meet these demands, satellite and payload manufacturers are using high-end FPGAs, ASICs, and processors. This paper discusses the power requirements of the Microchip® RTG4™ FPGA, which is being used to meet these high processing requirements, and how Renesas' comprehensive portfolio of radiation hardened power management ICs including point-of-load (POL) regulators, LDO voltage regulators, sequencers, supervisors, and operational amplifiers are used to develop a best-in-class power solution for this FPGA.

Introduction

The RTG4™ by Microchip® is one of the latest radiation hardened FPGAs with proven flight heritage, SEU immunity, and qualified to QMLV. RTG4 FPGAs integrate Microchip's fourth-generation Flash-based FPGA fabric high-performance Serialization/Deserialization (SERDES) transceivers on a single chip while maintaining resistance to radiation-induced configuration upsets in the harshest radiation environments, such as space flight (LEO, MEO, GEO, HEO, and deep space), medical electronics, and nuclear power plant control.[1]

RTG4™ is a low-power FPGA that has comparable performance to commercial counterparts in demanding computing applications. RTG4™ requires a complex power solution with multiple low voltage supply rails with higher operating currents and need to meet power sequencing requirements to eliminate high inrush currents. Additionally, the power solution needs to be highly reliable and space qualified. Couple-in the need for more efficient and smaller, light-weight power solutions and Renesas is at the forefront developing leading edge radiation hardened power solutions that meet the demands for radiation hardened FPGAs, ASICs, and other processors of today.

RTG4 Power Supply Requirements

Power Supply Rails

There are three main rails required for the FPGA, these are for the core voltage (VDD), the charge pumps (VPP), and for the I/O banks (VDDIx). Depending on the configuration and what devices the FPGA needs to interface with, the I/O rail can be different voltages ranging from 1.2V to 3.3V. The SerDes portion of the FPGA also requires three rails. One for its analog I/O voltage (SERDES_x_ Lyz_VDDAIO), another for the SerDes internal phase locked loops (SERDES_x_Lyz_VDDAPLL), and one for the clock receiver supply (SERDES_VDDI). In addition, there is the

VDDPLL rail that powers the PLLs used on the FPGA, DRAM memory, and PCIe/PCS rails. Finally, there is a SerDes reference voltage that is 50% of the SerDes clock receiver supply.

Recommended Operating Conditions

Table 1 summarizes the recommended operating voltages. This information was taken from the RTG4 FPGA datasheet.[2]

Table 1. Recommended Operating Voltage for the RTG4 FPGA

Symbol	Parameter	Min	Typ	Max	Units
VDD	DC FPGA core supply voltage. Must always power this pin.	1.14	1.2	1.26	V
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin	3.15	3.3	3.45	V
VDDPLL	Power for eight corner PLLs, PLLs in SerDes PCIe/PCS blocks, and FDDR PLL.	3.15	3.3	3.45	V
SERDES_x_ Lyz_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for Lane-y and Lane-z of SERDES_x. It is a +1.2V SerDes PMA supply.	1.14	1.2	1.26	V
SERDES_x_ Lyz_VDDAPLL	Analog power for SERDES_x PLL lanes y/z. It is a +2.5V SerDes internal PLL supply.	2.375	2.5	2.625	V
SERDES_VDDI	Power for SerDes reference clock receiver 1.8V supply. Must always power this pin.	1.71	1.8	1.89	V
	Power for SerDes reference clock receiver 2.5V supply. Must always power this pin.	2.375	2.5	2.625	V
	Power for SerDes reference clock receiver 3.3V supply. Must always power this pin.	3.15	3.3	3.45	V
SERDES_VREF	Reference voltage for SerDes receiver reference clocks.	0.49 × SERDES_ VDDI	0.5 × SERDES_ VDDI	0.51 × SERDES_ VDDI	V
VDDIx	1.2V DC supply voltage for FPGA I/O Banks	1.14	1.2	1.26	V
	1.5V DC supply voltage for FPGA I/O Banks	1.425	1.5	2.625	V
	1.8V DC supply voltage for FPGA and JTAG I/O Banks	1.71	1.8	1.89	V
	2.5V DC supply voltage for FPGA and JTAG I/O Banks	2.375	2.5	2.625	V
	3.3V DC supply voltage for FPGA and JTAG I/O Banks	3.15	3.3	3.45	V
	DC supply voltage for LVDS25 differential I/O Banks	2.375	2.5	2.625	V
	DC supply voltage for LVDS33 differential I/O Banks	3.15	3.3	3.45	V
	DC supply voltage for BLVDS, MLVDS, Mini-LVDS, RSDS differential I/O Banks	2.375	2.5	2.625	V
	DC supply voltage for LVPECL differential I/O Banks	3.15	3.3	3.45	V

Power Sequencing Requirements

There are two power-up supply sequencing requirements that need to be met on the VDDPLL and SERDES_x_Lyz_VDDAIO rails, however, there is no power-up sequence required if the following conditions are met:

- The RTG4 is held in reset by asserting DEVRST_N until VDDPLL supplies reach their minimum recommended level
- The SERDES_x_Lyz_VDDAIO supplies are tied to VDD

If these conditions cannot be met, you must ensure that:

- VDDPLL is NOT the last supply to ramp up and must reach its minimum recommended level before the last supply (VDD or VDDIx) starts ramping up.
- If SERDES_x_Lyz_VDDAIO and VDD cannot be tied together, SERDES_x_Lyz_VDDAIO must be powered up at the same time as VDD.

No power-down sequence is needed if an external 1kΩ pull-down resistor is used for each critical output, which cannot tolerate an output glitch during power-down or DEVRST_N assertion. If an external resistor cannot be used, either of the following requirements apply.

- VDDIx supplies are powered down first all the way to 0V.
- VPP is powered down last.

RTG4 FPGA Development Kit

Development Kit Overview

Microchip's RTG4 development platform allows you to protype and evaluate the performance of the FPGA in different applications. Figure 1 shows a block diagram of the development board. The board includes two 1GB Double Data Rate 3 (DDR3) memories and two 1GB SPI flash memories. The board also has several standard and advanced peripherals, such as PCIe x4 edge connector, two FMC connectors for using several off-the-shelf daughter cards, USB, Philips inter-integrated circuit (I^2C), gigabit Ethernet port, serial peripheral interface (SPI), and UART. Additionally, a FlashPro programmer is embedded on the board, which allows RTG4 FPGA programming through the JTAG interface[3].

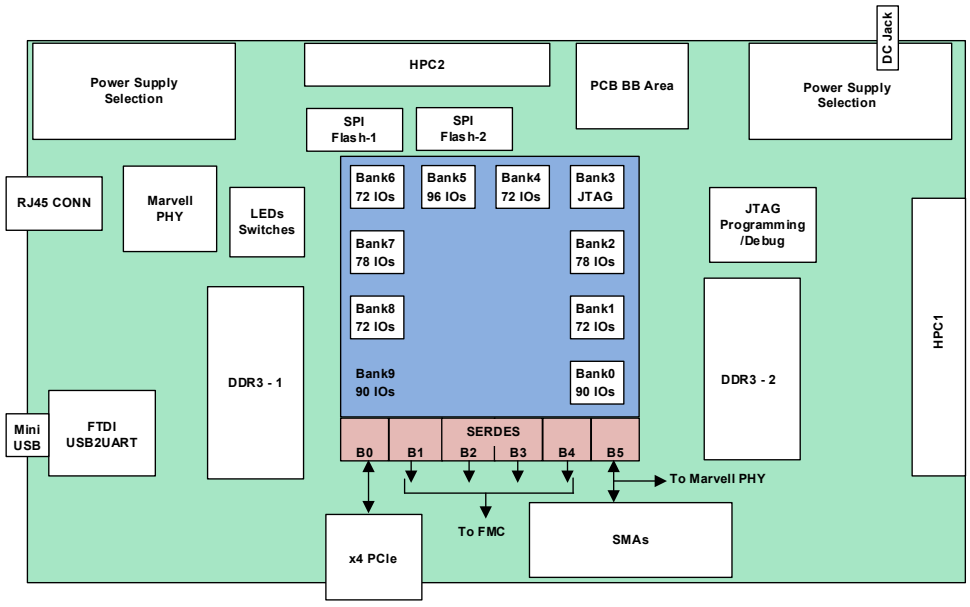

Figure 1. Block Diagram of the RTG4 Development Kit

Development Kit Power Solution

Figure 2 shows a block diagram of the power solution used on the development board. A total of 13 voltage regulators generate all the necessary voltage to power the digital loads. The main input is a 12V DC that is controlled by an ON/OFF switch. In the ON position, the 12V input voltage feeds three regulators to generate 1.2V, 3.3V, and 5V voltage rails. The 1.2V powers the core VDD rail of the FPGA directly. The 3.3V and 5V are intermediate bus voltages distributed around the board and used as inputs to other POLs and LDOs for further conversion.

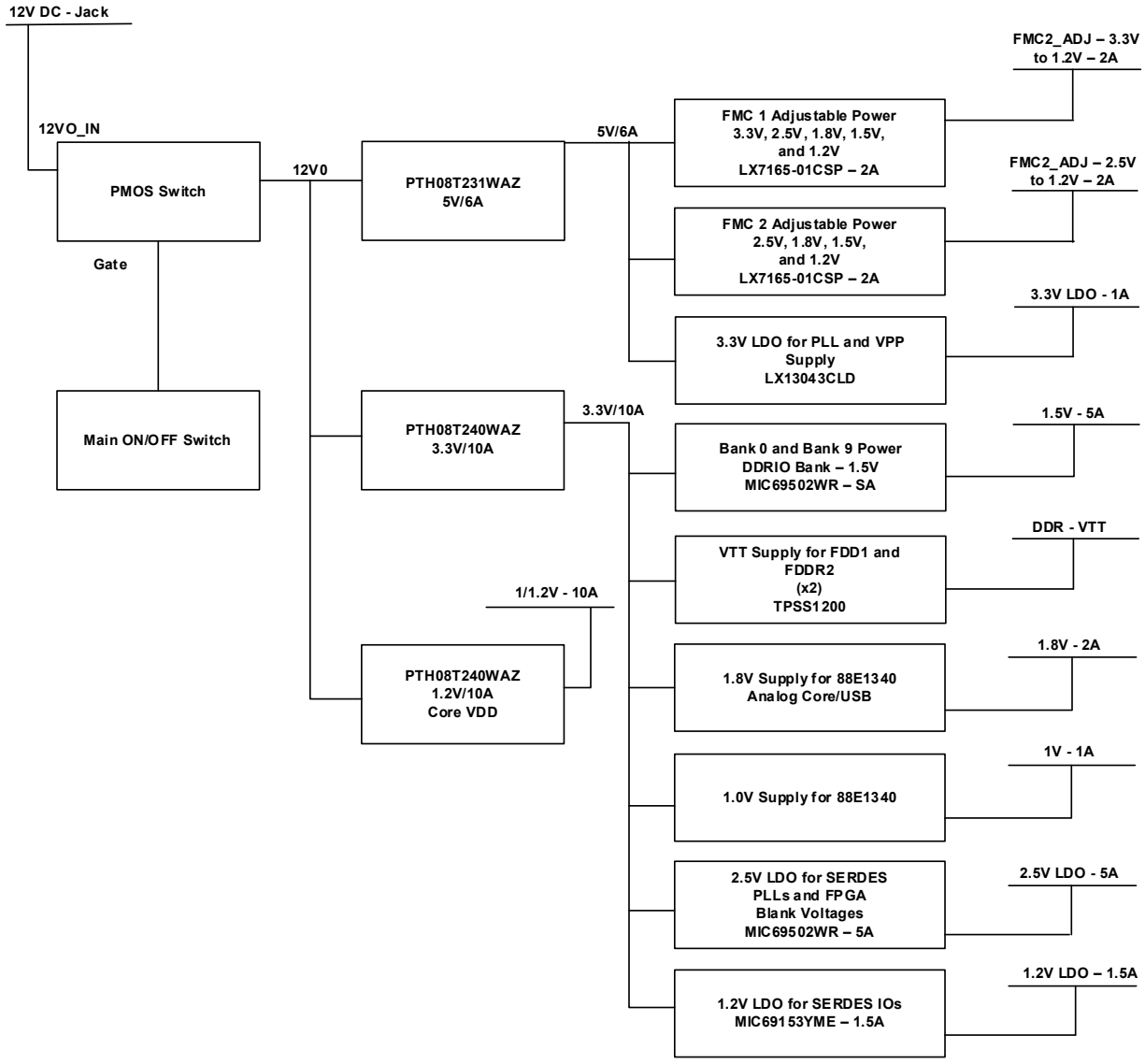

Figure 2. Block Diagram of the Power Tree for the RTG4 Development Kit

Renesas' Space Grade Power Solution

Figure 3 shows a space grade power solution for the RTG4 development board using six unique products (shaded blue blocks) from Renesas' broad portfolio of radiation hardened power management and analog ICs.

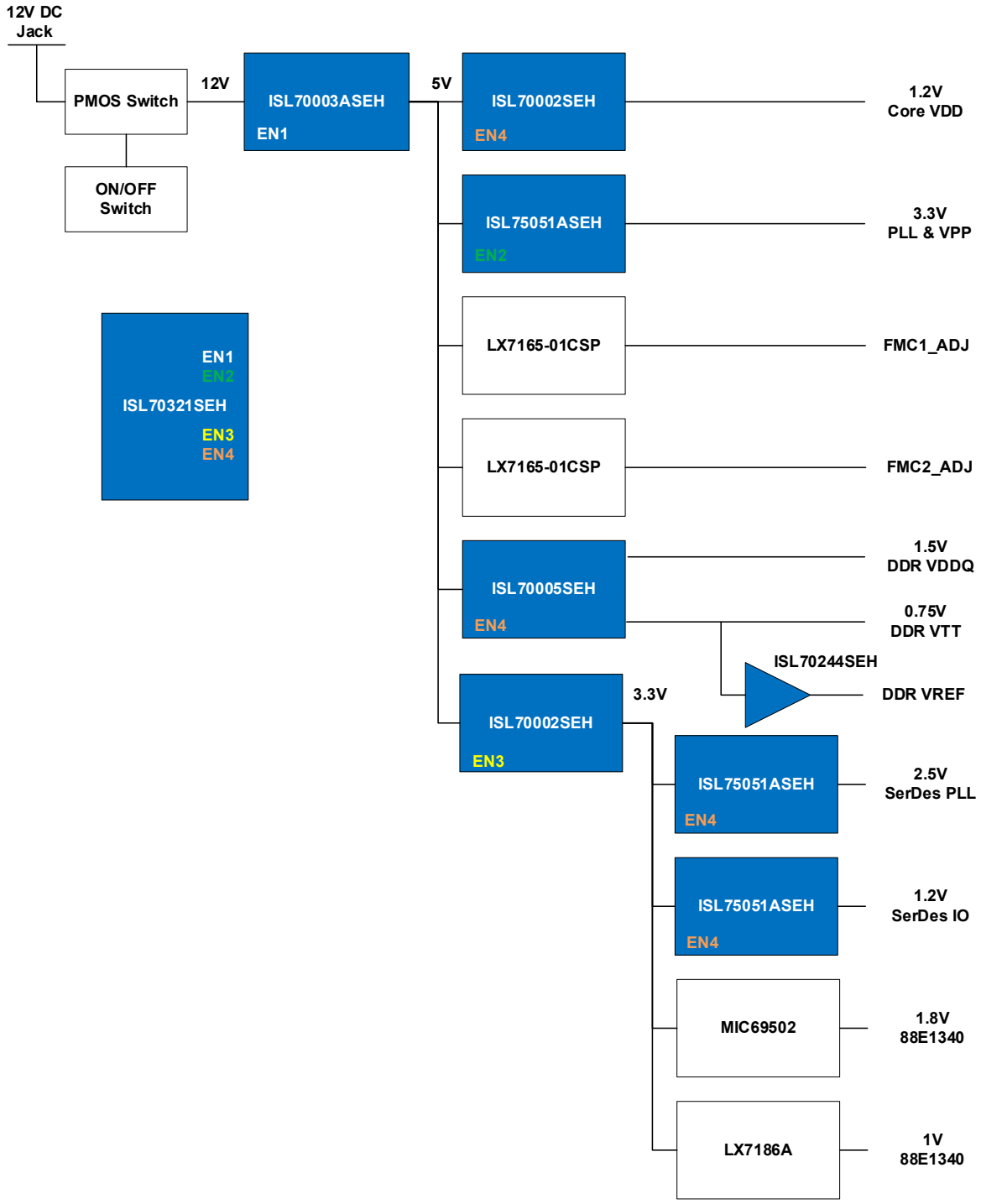

Figure 3. Renesas' Space Grade Power Solution for the RTG4 Development Kit

Table 2 summarizes the part number, description, and operating conditions of the POLs and LDOs used in the space grade design.

Table 2. Radiation Hardened Power Management IC Configuration

Part Number	Description	Input	Output Name	Output	Load
ISL70003ASEH	Radiation and SEE Tolerant 3V to 13.2V, 9A Buck Regulator	12V	5V Intermediate Rail	5V	9A
ISL70002SEH	Radiation Hardened and SEE Hardened 22A Synchronous Buck Regulator with Current Sharing	5V	VDD Core	1.2V	16A
ISL75051ASEH	Power for eight corner PLLs, PLLs in SerDes PCIe/PCS blocks, and FDDR PLL.	5V	VDDPLL & VPP	3.3V	1A
ISL70005SEH	Radiation Hardened Dual Output Point-of-Load, Integrated Synchronous Buck and Low Dropout Regulator	5V	DDR VDDQ	1.5V	3A
		1.5V	DDR VTT	0.75V	±1A
ISL70002SEH	Radiation Hardened and SEE Hardened 22A Synchronous Buck Regulator with Current Sharing	5V	3.3V Intermediate Rail	3.3V	10A
ISL75051ASEH	3A, Radiation Hardened, Positive, Ultra-Low Dropout Regulator.	3.3V	SERDES_x_ Lyz_VDDAIO	1.2V	3A
ISL75051ASEH	3A, Radiation Hardened, Positive, Ultra-Low Dropout Regulator	3.3V	SERDES_x_ Lyz_VDDAPLL	2.5V	2A

In addition to the power management ICs, the ISL70321SEH quad power supply sequencer controls the power-up and power-down sequences of the power system. Figure 3 color codes the connections from the ISL70321SEH enable output to the enable input of the various power management ICs.

The following list summarizes the monitoring and control function of the ISL70321SEH:

- The 12V DC voltage is monitored by the ISL70321SEH and enables the ISL70003ASEH first when the voltage after the PMOS switch reaches 10V.
- When the 5V intermediate rail is up, the ISL75051ASEH is enabled to power the VPLL & VPP rail.
- When the VPLL & VPP rail is above the 3.1V, the ISL70002SEH is enabled to generate the 3.3V intermediate rail.
- When 3.3V is up, the regulators for the core VDD, DDR memory, and SerDes are enabled simultaneously.
- When the VDD rail is in proper regulation, the DONE signal from the ISL70321SEH is asserted high, which releases the RESET signal to the FPGA.

The final IC used in the power solution is the ISL70244SEH, a 19MHz radiation hardened 40V dual rail-to-rail input-output, low-power operational amplifier. It generates the DDR reference voltage in a buffer configuration with its input connected to the LDO output of the ISL70005SEH to achieve 50% tracking of the VDDQ rail.

Note: No changes have been made to the regulators for the FMC connectors or Ethernet PHY ICs.

ISLRTG4DEMO1Z Reference Board

With permission from Microchip and in collaboration with Ibeos, the RTG4 development board schematic and layout board were modified to replace its power solution with the one proposed in Figure 3. An image of the ISLRTG4DEMO1Z reference board is shown in Figure 5. It has the same functionality as the Microchip RTG4 Development Kit but includes the space grade power solution.

The schematic and the Gerber files for the board are available on the applicable device pages. You can use these files as a starting point or use them directly in their own designs.

To verify functionality, demo programs that are available from Microchip were loaded and ran on the board successfully. Additionally, a scope shot for the power-up sequence of the reference board is shown on Figure 4.

The top trace of the scope shot includes the control signal on the UP/INIT pins of the ISL70321SEH power supply sequence. This signal comes from resistor divider connected to the main 12V power source applied with the DC jack. The resistor combination enables the sequencer when the main power source reaches 10V.

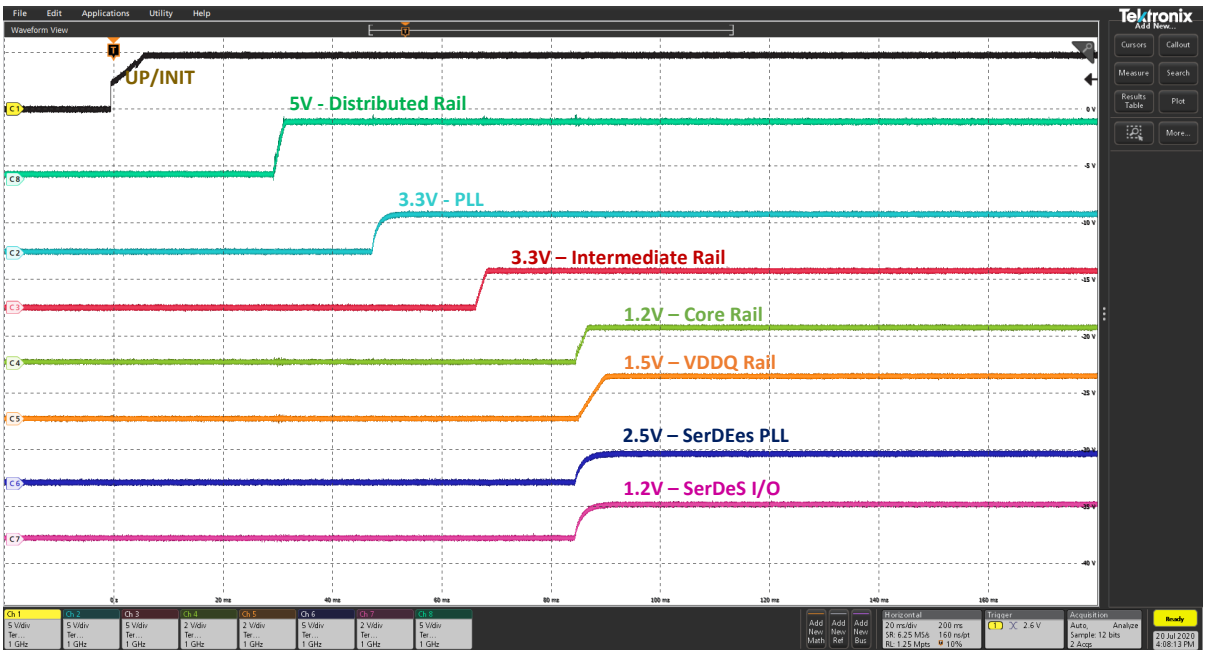

Figure 4. Power Up Sequence of the RTG4 Reference Design

The rest of the traces on Figure 4 are the output voltages of the POLs and LDOs that are controlled by the ISL70321SEH. See the block diagram in Figure 3, which color coordinates the enable outputs of the sequencer to the corresponding enable inputs of the regulators.

This is summary of the traces in order from top to bottom, found in Figure 4:

1. UP/INIT signal to enable power-up sequence
2. Distributed 5V rail, generated by the ISL70003ASEH
3. 3.3V for the PLLs generated by the ISL75051ASEH
4. Intermediate 3.3V rail generated by the ISL70002SEH
5. 1.2V core rail generated by the ISL70002SEH

6. 1.5V, VDDQ rail for DDR memory generated by the buck portion of the ISL70005SEH

7. 2.5V SerDes PLL rail generated by the ISL75051ASEH

8. 1.2V SerDes I/O rail generated by the ISL75051ASEH

Because there are no power-down requirements on the RTG4 FPGA, the reference boards are set up to disable all regulators at the same time when the power switch is turned to the OFF state.

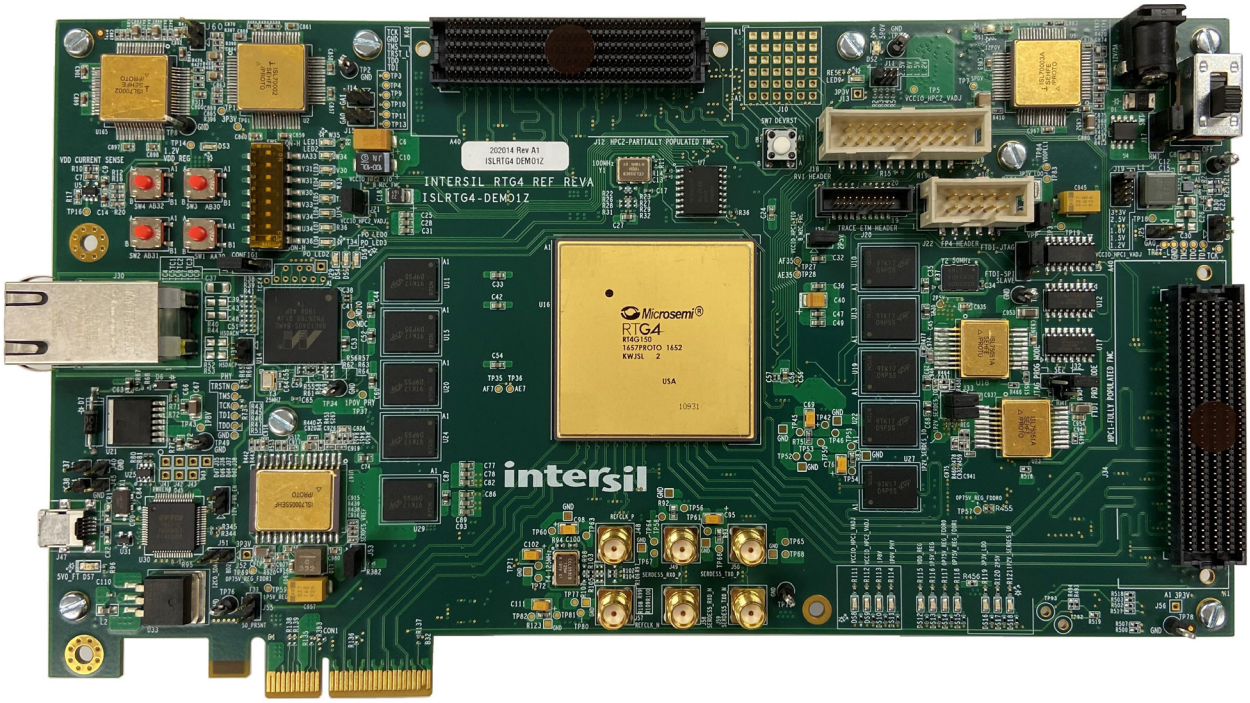

Figure 5. Renesas' RTG4 Reference Board

Conclusion

As satellites and spacecraft manufacturers use more high-density, high-processing, and reprogrammable FPGAs such as the Microchip® RTG4™, the power solutions must also be high-performance and robust to meet the requirements of the FPGA. This paper discussed how Renesas' space grade power management and analog products make it easy for you to achieve a highly reliable and efficient power solution for the RTG4 FPGA. Successful operation was verified by running the demonstration programs made available by Microchip. Power sequencing and fault protection was achieved with the ISL70321SEH quad power supply sequencer, which offers a more reliable solution than using the PGOOD and soft-start functions of the POL or LDO.

The outcome is a full reference design featuring a reliable and efficient power solution that has been fully validated. Additionally, all the necessary files are available for the ISLRTG4DEMO1Z for you to use as-is in your system, alleviating the hassle of designing the power supply.

Next Steps

- **Learn more about the ISL70003ASEH**
- **Learn more about the ISL75051ASEH**
- **Learn more about the ISL70002SEH**
- **Learn more about the ISL70005SEH**
- **Learn more about the ISL70321SEH**
- **Learn more about the ISL70244SEH**

References

1. RTG4 Radiation-Tolerant FPGAs Product Overview, https://www.microsemi.com/product-directory/rad-tolerant-fpgas/3576-rtg4#overview
2. RTG4 FPGA Datasheet, DS0131 Datasheet Revision 6.0, https://www.microsemi.com/document-portal/doc_download/135193-ds0131-rtg4-fpga-datasheet
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